https://ucberkeleyee290c.github.io/sp22/

EE290C: 28nm SoC for IoT

Analog Layout and Matching

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- Please do not post these slides on the Internet. There are no "secrets" in these slides, but they contain some actual layouts from my consulting.

Topics

Part 1

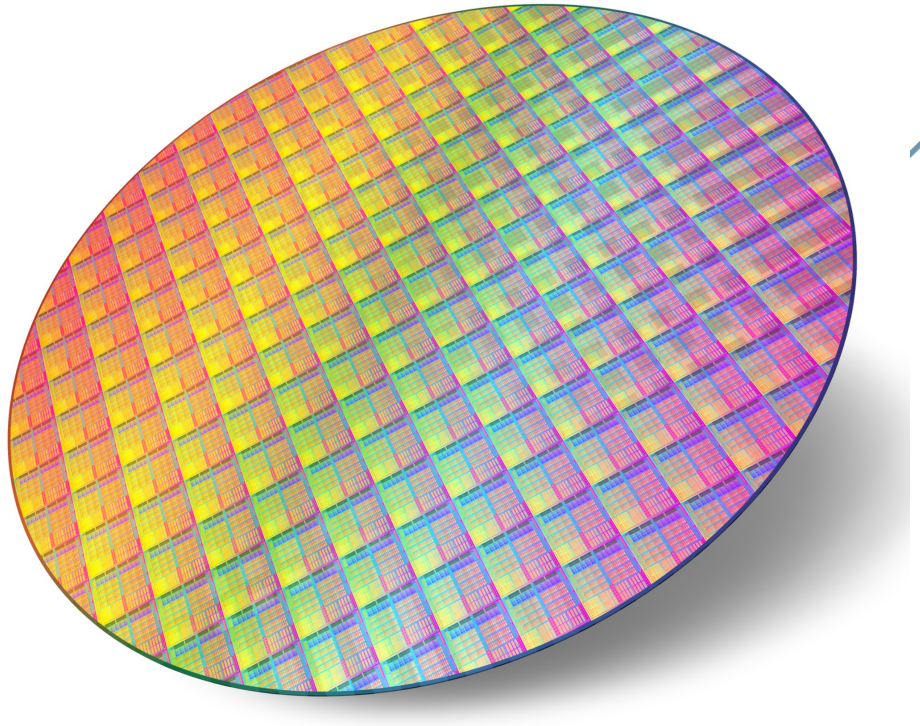
- Analog Layout
  - Matching
  - Common centroid
  - Symmetry
  - Unit Cell Concept
- Current Source
- Differential Pair

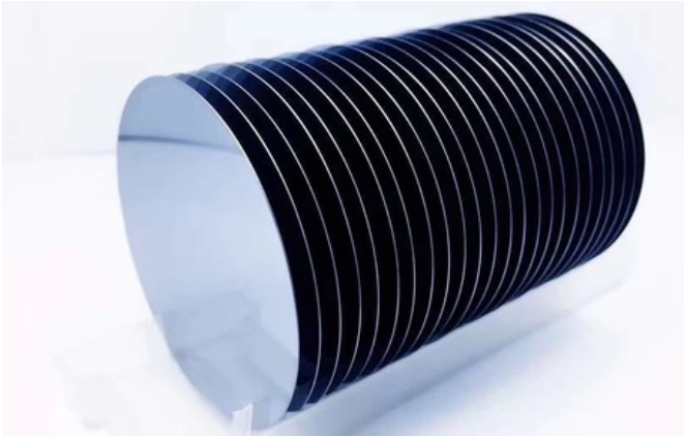
Part 2

- Capacitors
  - Love your MOM
- Resistors
- More arrays
- Inductors
- Electromigration Rules
- Antenna Rules
- Examples:
  - DAC
  - Op-Amp
  - Tiles of blocks
  - Pin placement
- Layout Hierarchy vs Schematic

Matching

- Systematic Offsets – can usually fix with good layout
- Wafer-to-wafer variations, lot-to-lot, die-to--die, and transistor-to-transistor !
- Process Induced “Global” Mismatch – all transistors experience the same variations (say VTH), similar to “corner sims”
  - FF, FS, SF, SS, TT
- Process Induced “Local” Mismatch
  - Even two transistors on the same die sitting next to each other will be slightly different !
  - VTH mismatch

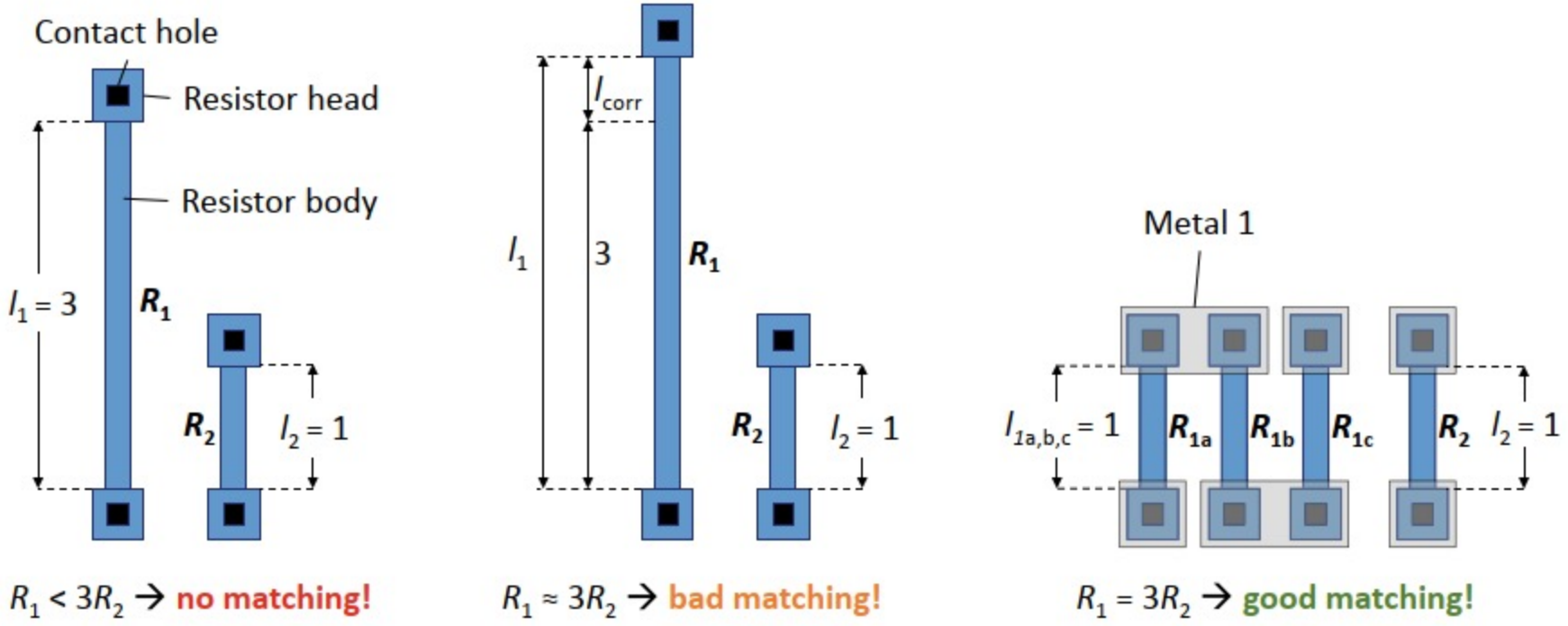




Mismatch Between Transistors

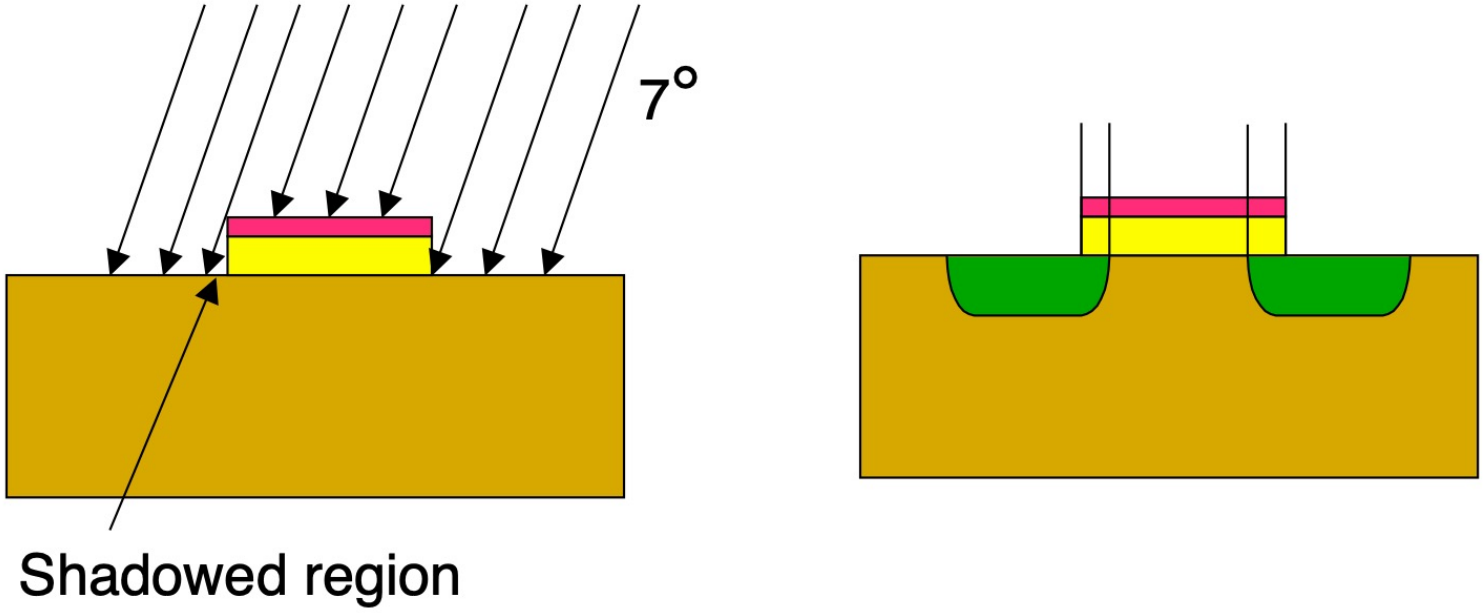
- Systematic offset (metal on top or different environment)
  - Eliminate this component as much as possible
- Geometry
  - Line edge roughness
  - Avoid minimum sized structures
- Doping
  - Threshold voltage implant
  - Avoid small transistors
  - A given W/L can be realized with a non-minimum sized device

Matching: Resistors Example



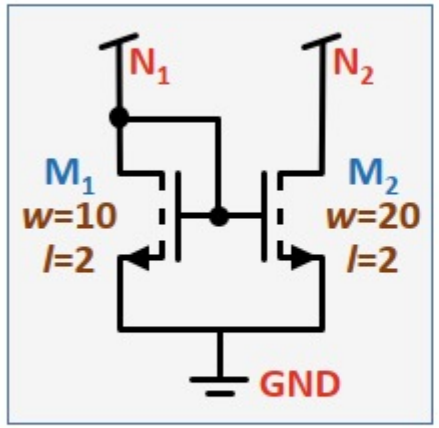
Lienig, Scheible, "Fundamentals of Layout Design for Electronic Circuits," Springer 2020.

Asymmetry due to Fabrication

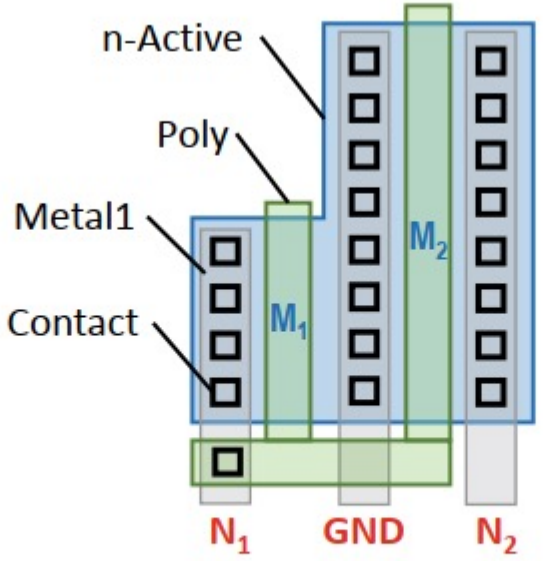


- Implants are tilted by 7 degrees
- Source and Drain are not Symmetric !

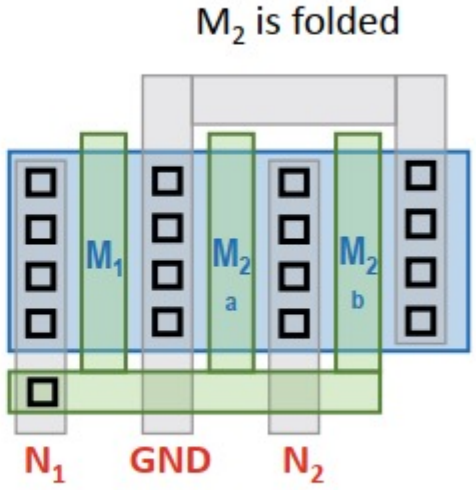
Matching: MOS Current Mirror



Current mirror circuit



No splitting → bad matching!



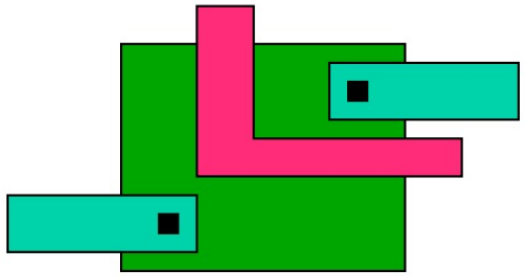
Splitting → good matching!

Better matching

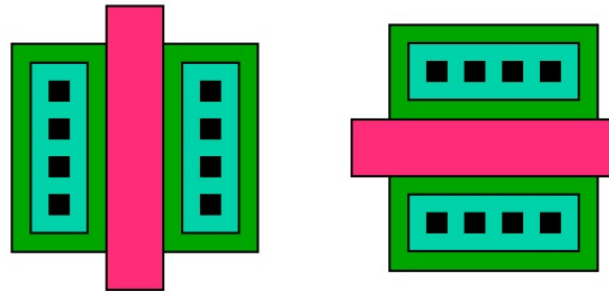
Lienig, Scheible, "Fundamentals of Layout Design for Electronic Circuits," Springer 2020.

Multiple Single Transistors

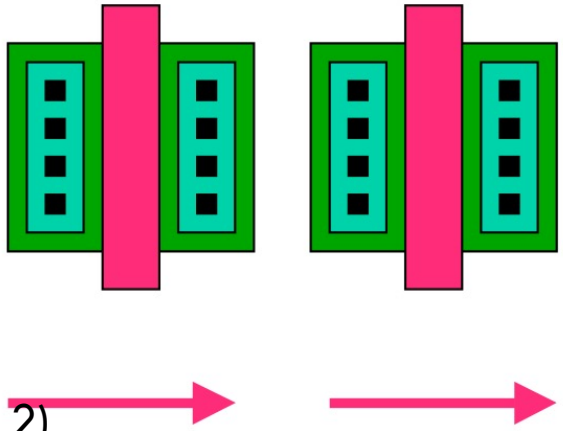
- Use Regular Rectangular Shapes



- Use Parallel Elements
  - Direction matters with Silicon



- Try to have current flow in the same direciton



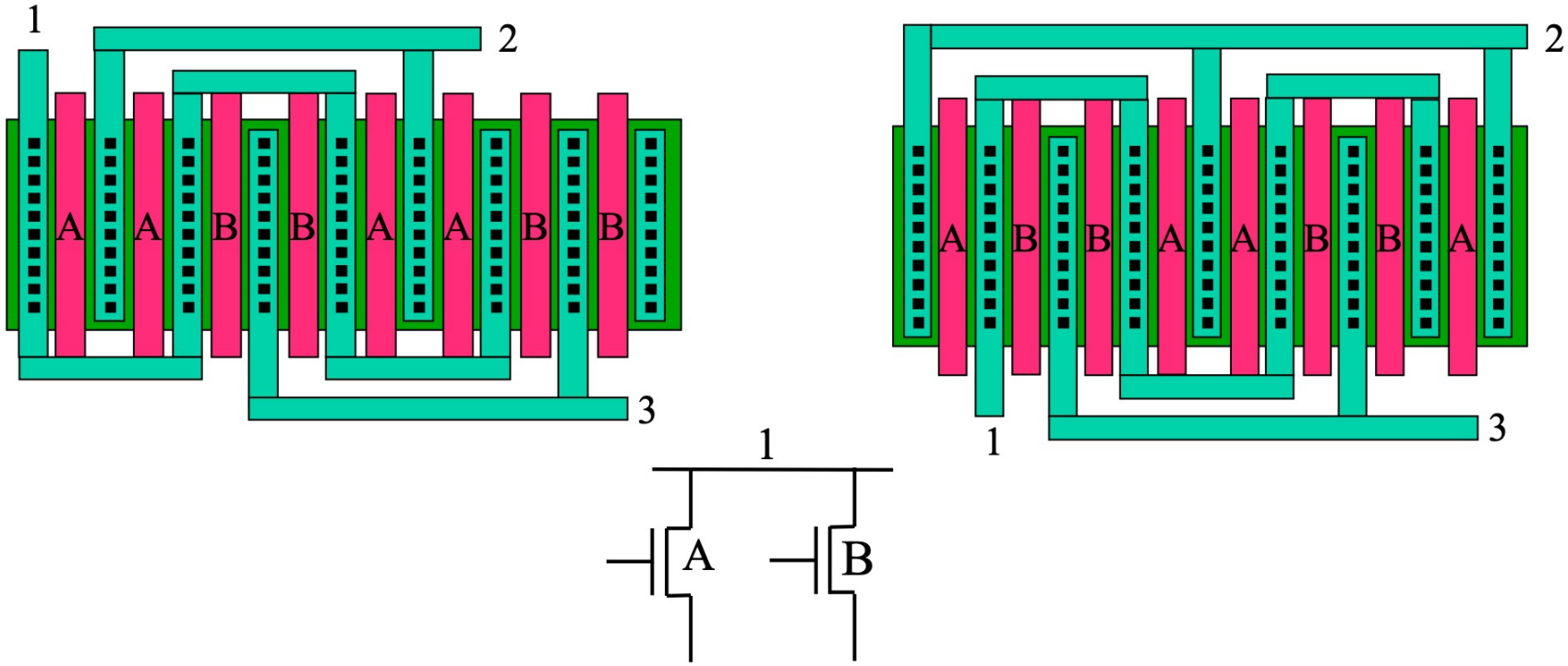
Maloberti, F, “Layout of Analog CMOS Integrated Circuits” (Part 2)

Layout Patterns

- Translational Symmetry versus Reflection
- Beautiful is not always better !
- When matching, keep everything the same as much as possible
- Assume up and down and left and right are asymmetric !

Interdigitated Devices

- Two matched transistors are laid out together using one big interdigitated transistor
- Which pattern is better ? AABBAABB or ABBAABBA?



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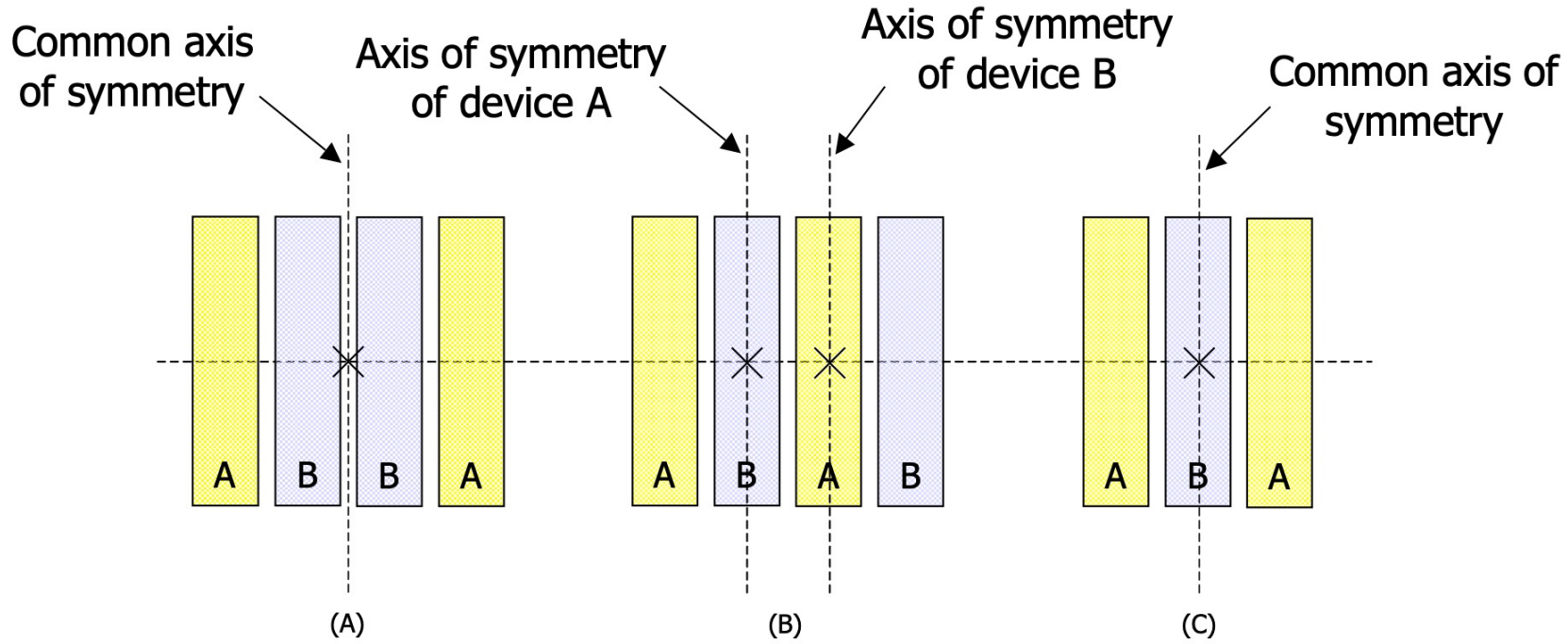
Axis of Symmetry



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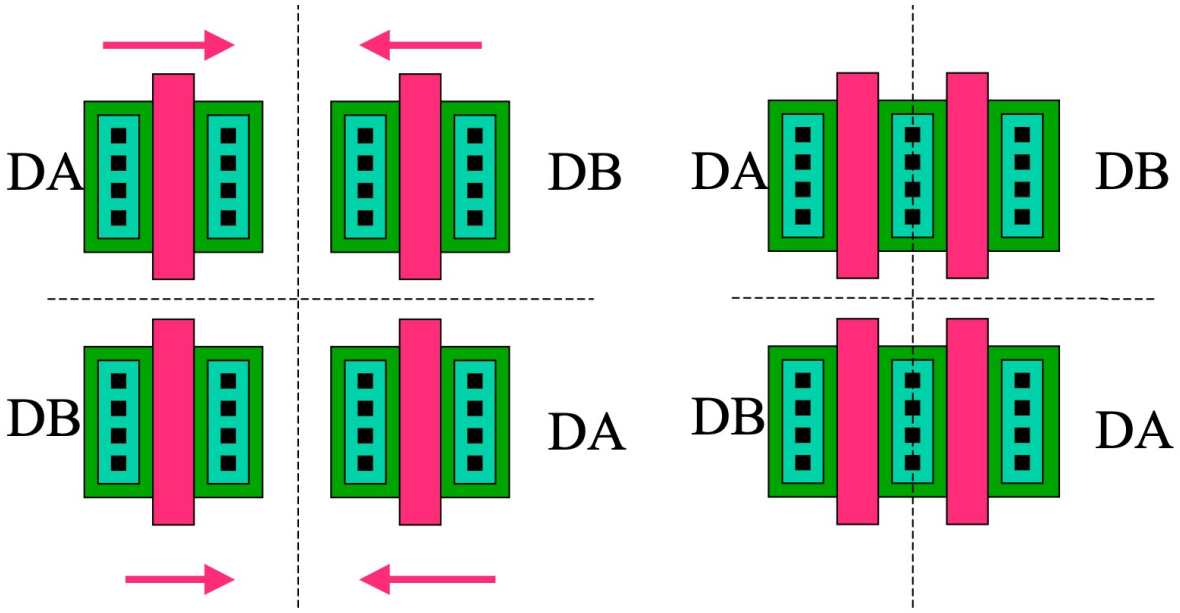
Common Centroid

- Using a common-centroid layout style, we can cancel gradients (to first order)



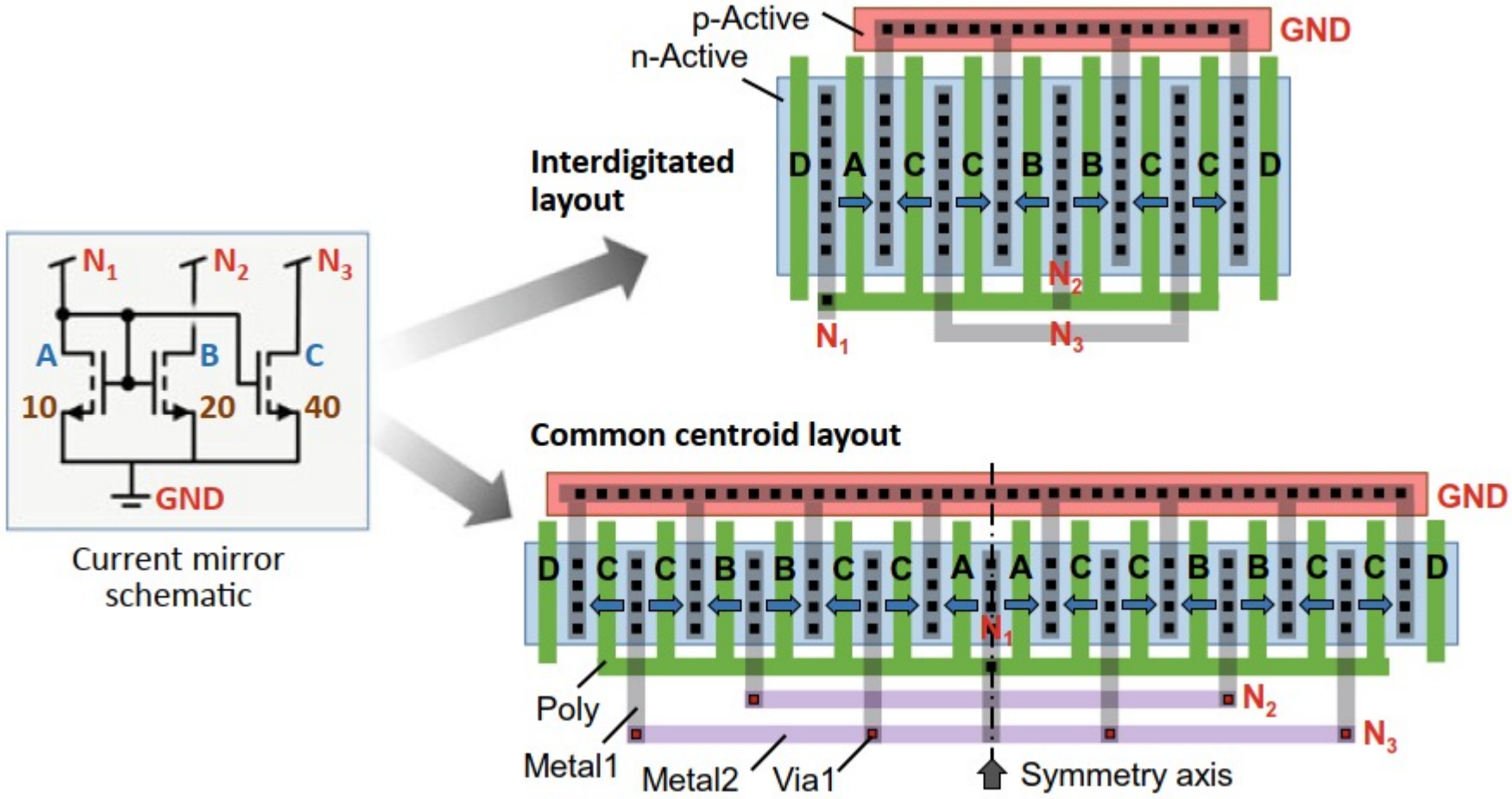
Maloberti, F, “Layout of Analog CMOS Integrated Circuits” (Part 2)

Interdigitation Patterns

- Can also stack transistors in vertical direction

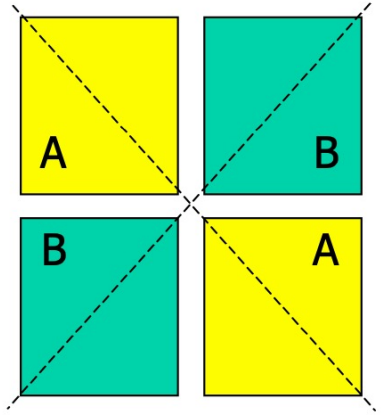
A	AA	AAA	AAAA
AB*	ABBA	ABBAAB*	ABABBABA
ABC*	ABCCBA	ABCBACBCA*	ABCABCCBACBA
ABCD*	ABCDDCBA	ABCBCADBCDA*	ABCDDCBAABCDDCBA
ABA	ABAABA	ABAABAABA	ABAABAABAABA
ABABA	ABABAABABA	ABABAABABAABABA	ABABAABABAABABAABABA
AABA*	AABAABAA	AABAAABAAABA*	AABAABAAAABAABAA
AABAA	AABAAAABAA	AABAAAABAAAABAA	AABAAAABAAAABAAAABAA

Common Centroid

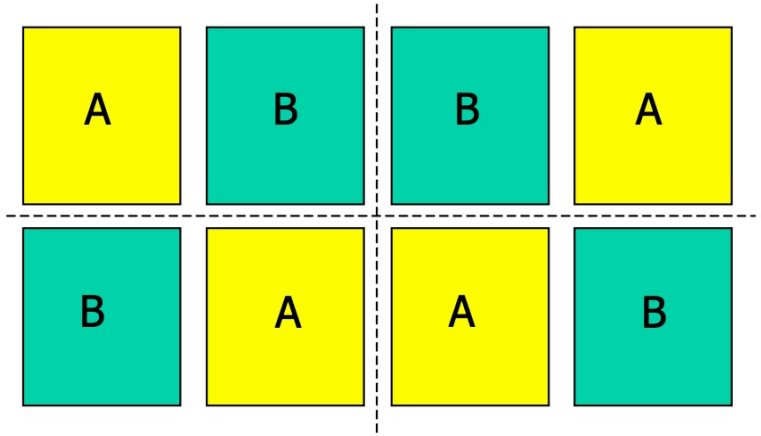


Lienig, Scheible, "Fundamentals of Layout Design for Electronic Circuits," Springer 2020.

Common Centroid Arrays



Cross coupling



Tiling (more sensitive to high-order gradients)

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Common Centroid Patterns

ABBA BAAB	ABBAABBA BAABBAAB	ABBAABBA BAABBAAB ABBAABBA	ABBAABBA BAABBAAB BAABBAAB ABBAABBA
ABA BAB	ABAABA BABBAB	ABAABA BABBAB ABAABA	ABAABAABA BABBABBAB BABBABBAB ABAABAABA
ABCCBA CBAABC	ABCCBAABC CBAABCCBA	ABCCBAABC CBAABCCBA ABCCBAABC	ABCCBAABC CBAABCCBA CBAABCCBA ABCCBAABC
AAB BAA	AABBAA BAAAAB	AABBAA BAAAAB AABBAA	AABBAA BAAAAB BAAAAB AABBAA

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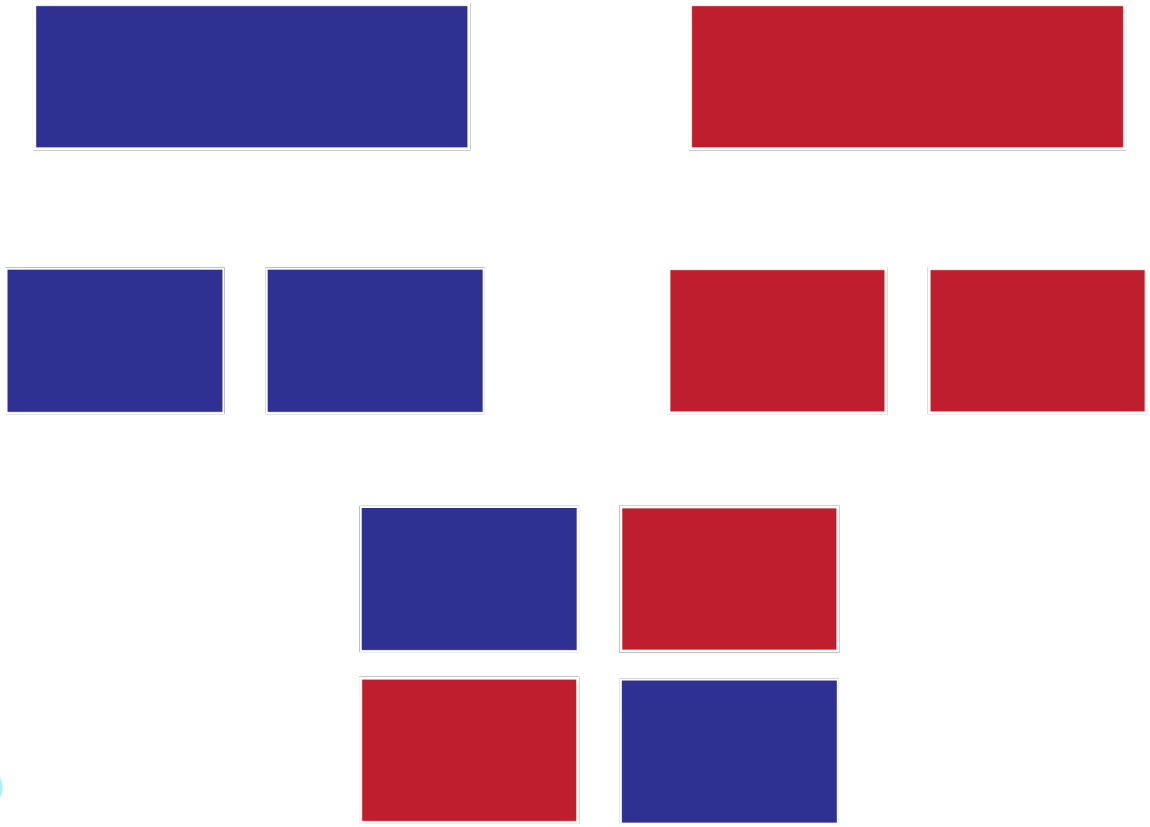
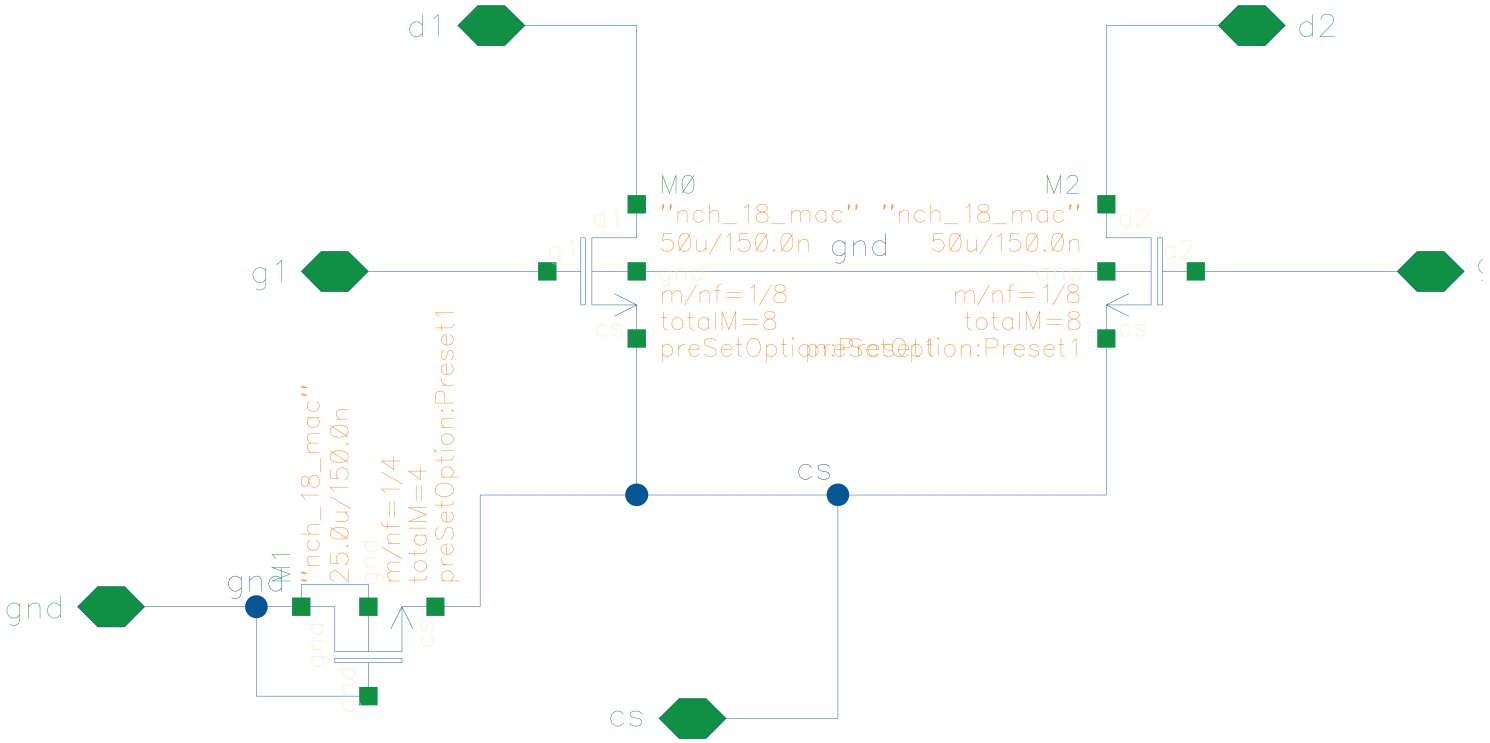
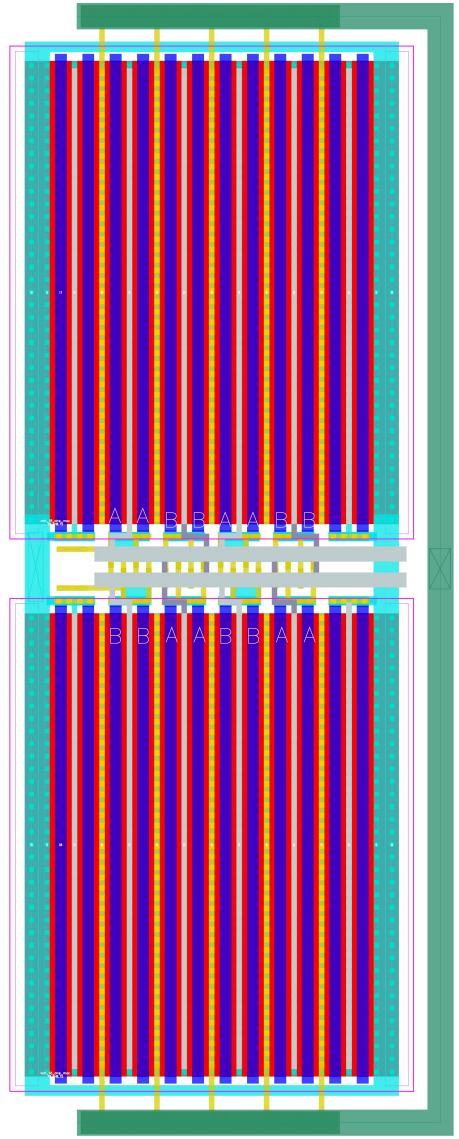
Example: Differential Pair



- Split transistors into smaller units
- Layout units in an array in a common centroid fashion
- Impossible to keep metal interconnections symmetric, so make sure IR drops are not an issue

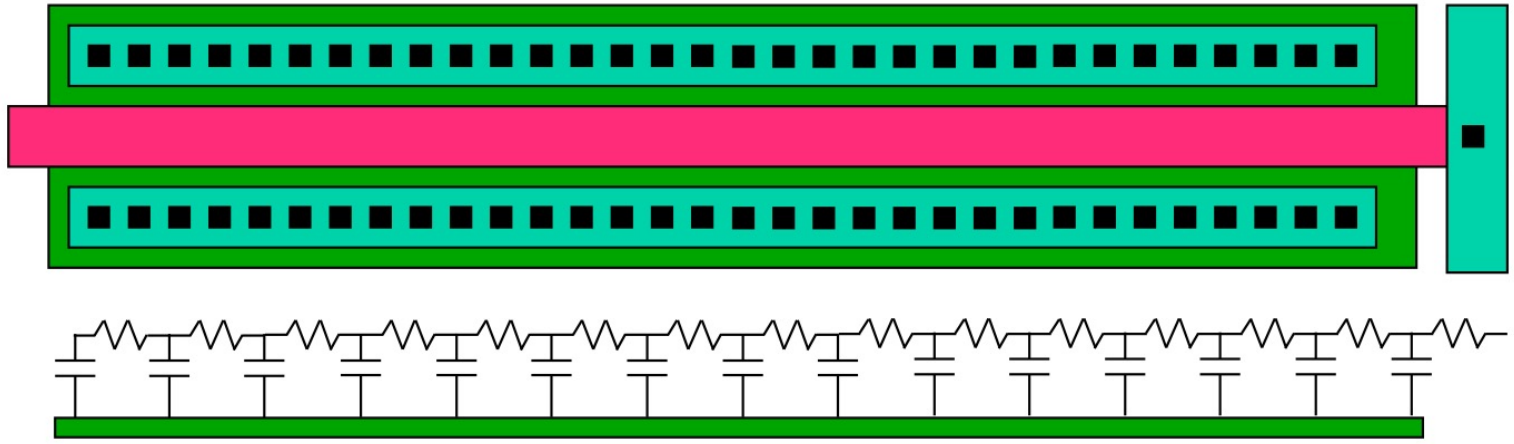
Layout Example: Differential Pair





Don’t forget about “IR” Drops

- Metals have considerable resistance since they are very narrow
- Poly is especially resistive
- Vias are tiny and introduce 10’s of ohms of resistance … use many in parallel
- Make sure I*R drops are small and for differential circuits, make it symmetric so it’s a common mode offset
- Use more fingers



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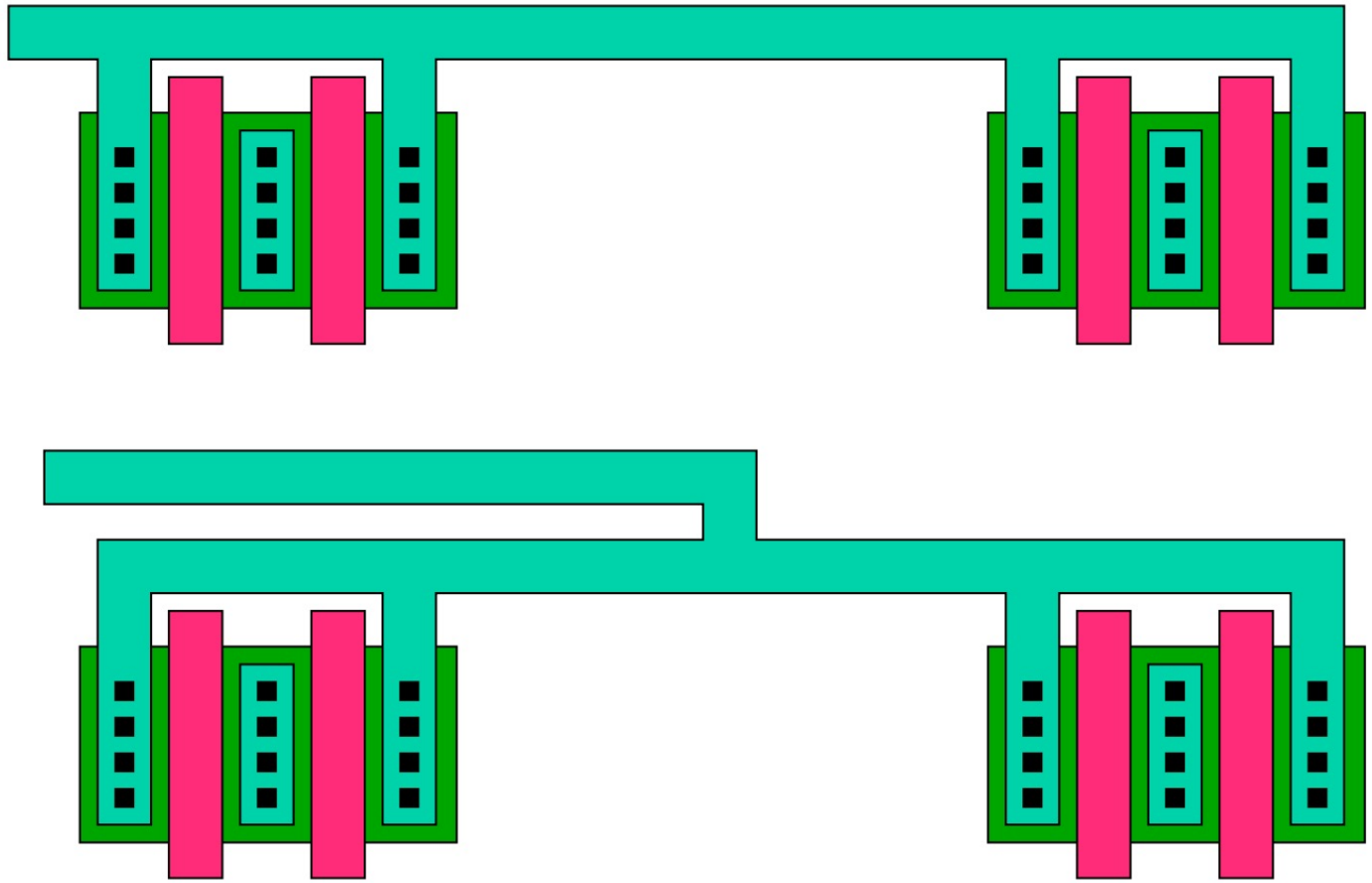
Matched Interconnect



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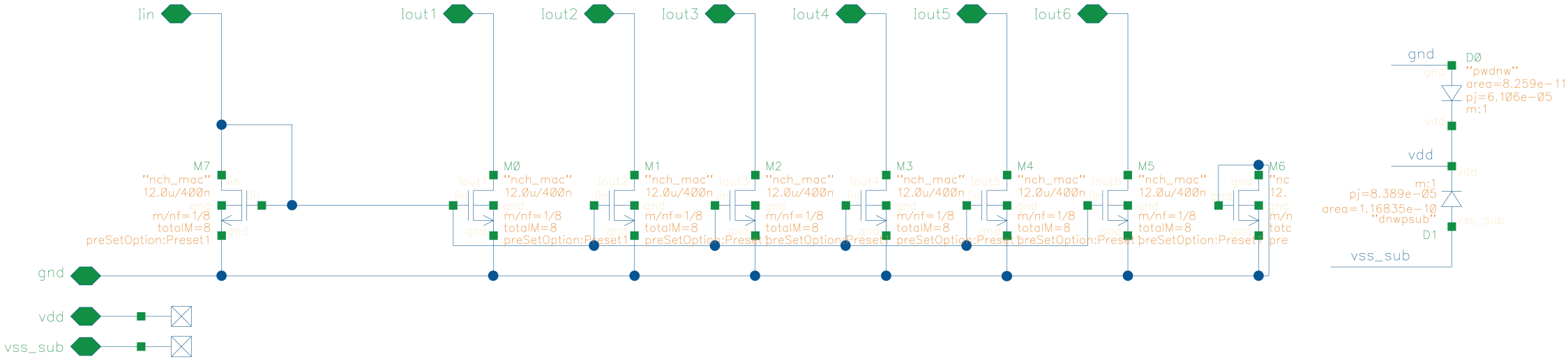
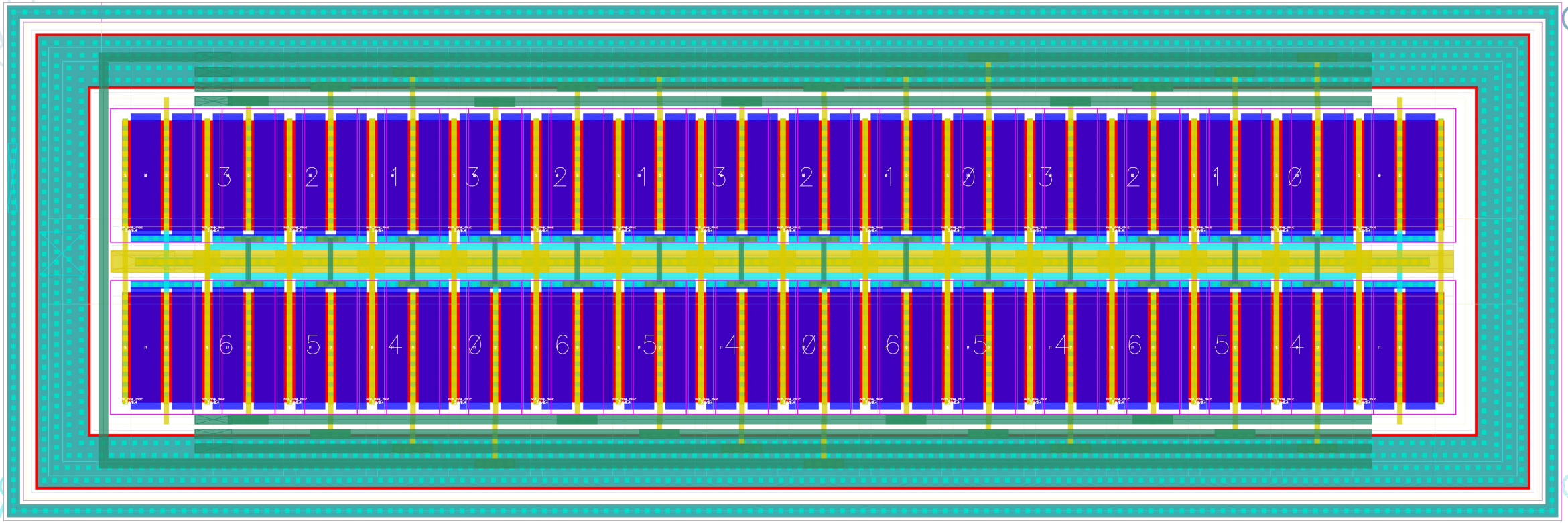
Real Life Examle: Current Source Distribution

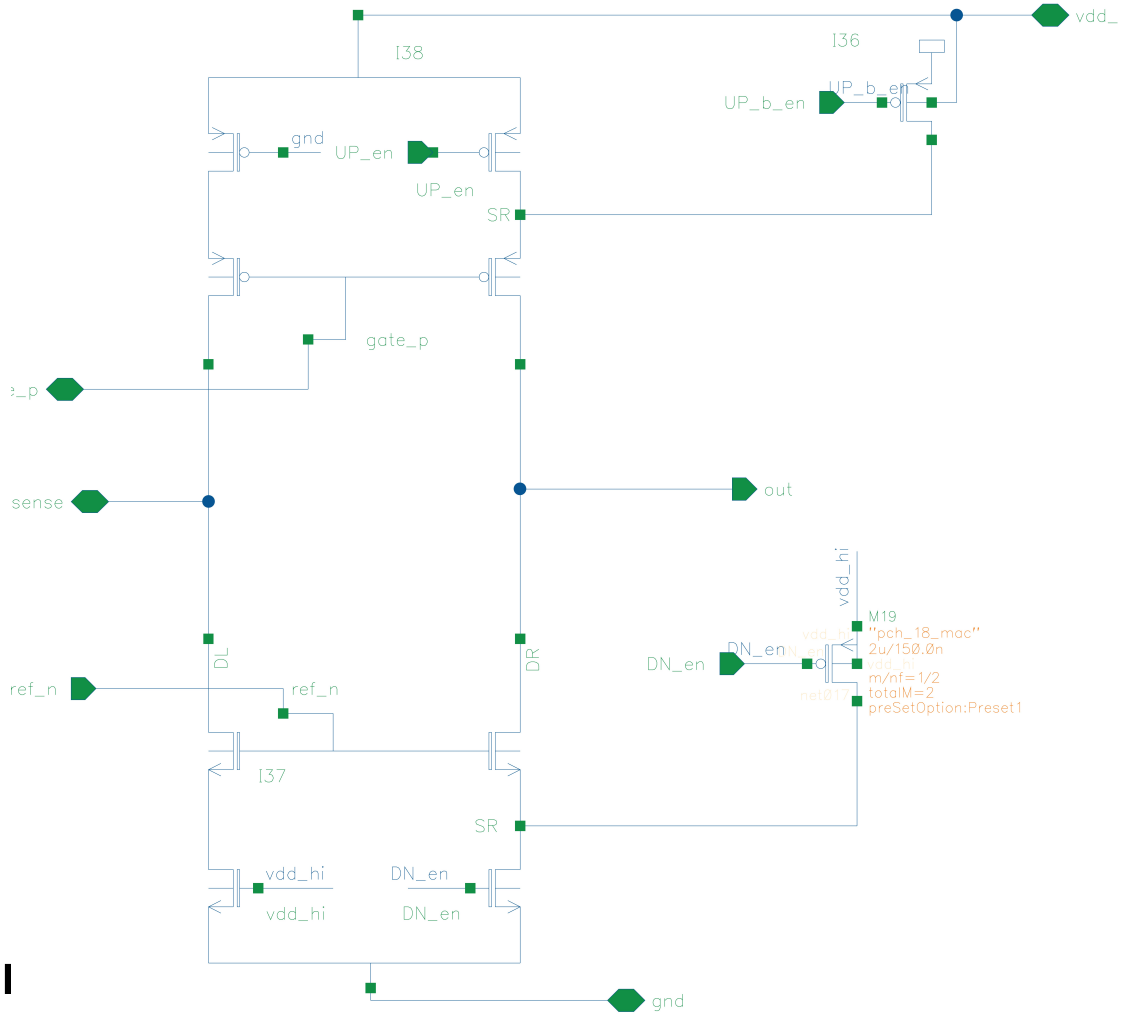


Multi-Output Current Source Layout

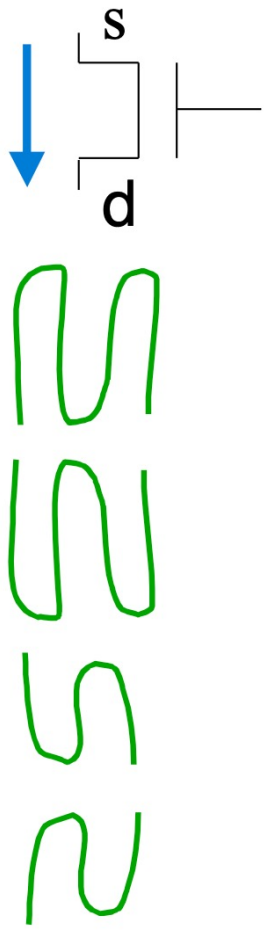


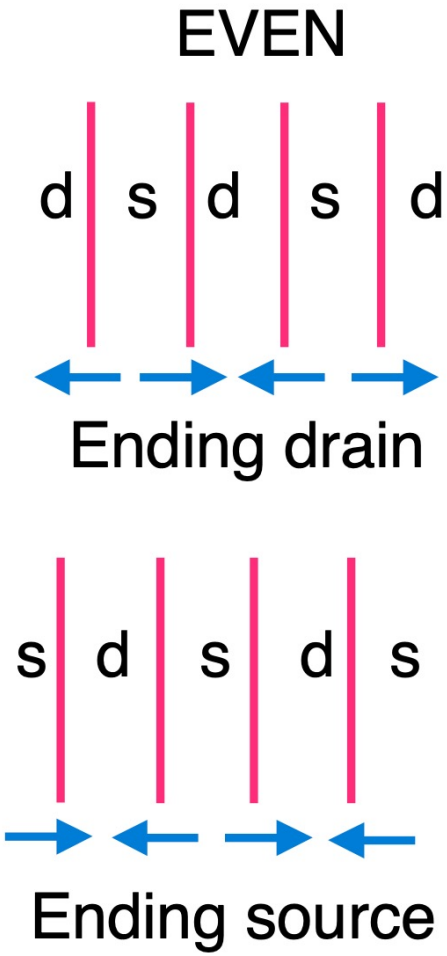
Stacked and Parallel Layout

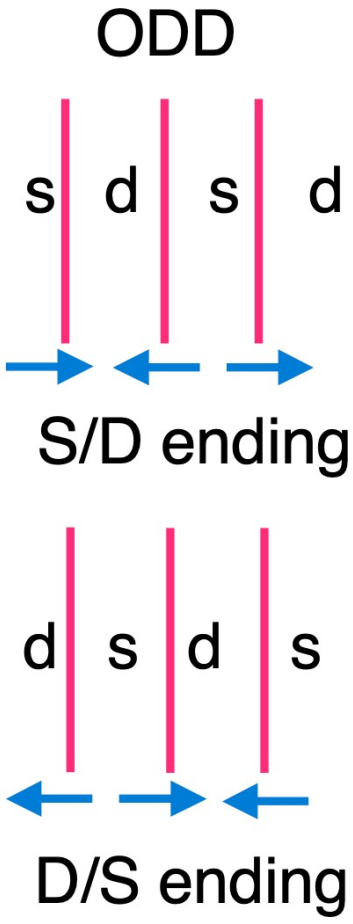
- When transistors are connected and share a junction (think of a current source, or a cascode connection), we can group them together
- To do this, the transistors need to have the same finger width
  - Modify your schematic so that all transistors are a multiple of a unit finger width, say 0.5um or 1um
- In the schematic, identify which transistors can be grouped together



Odd/Even Fingers and S/D Swaps







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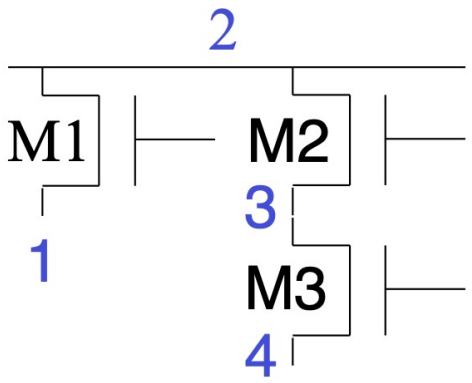
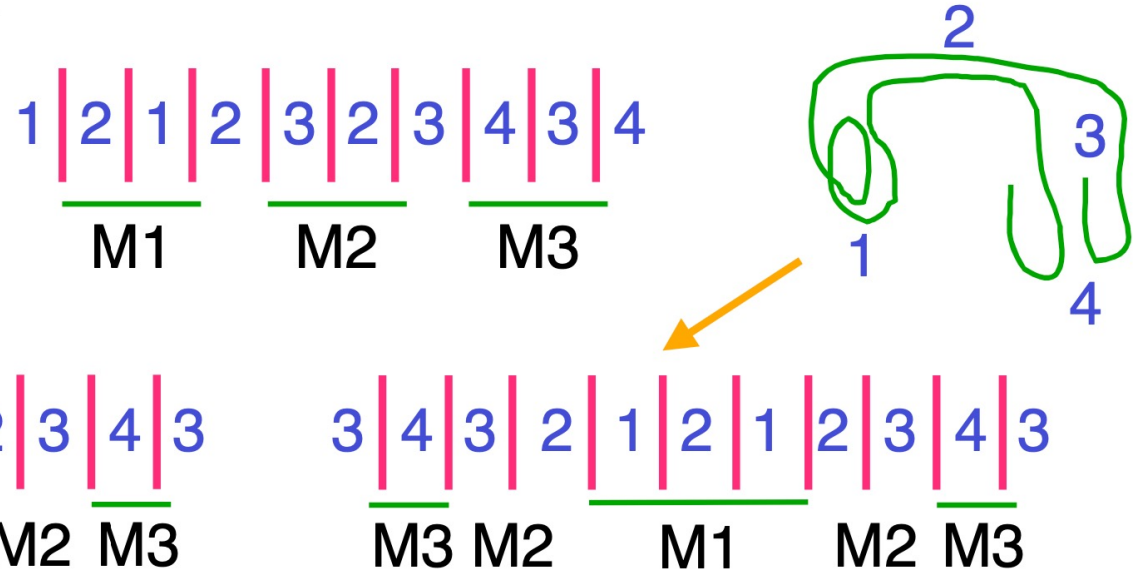
Example of Stacking and Grouping





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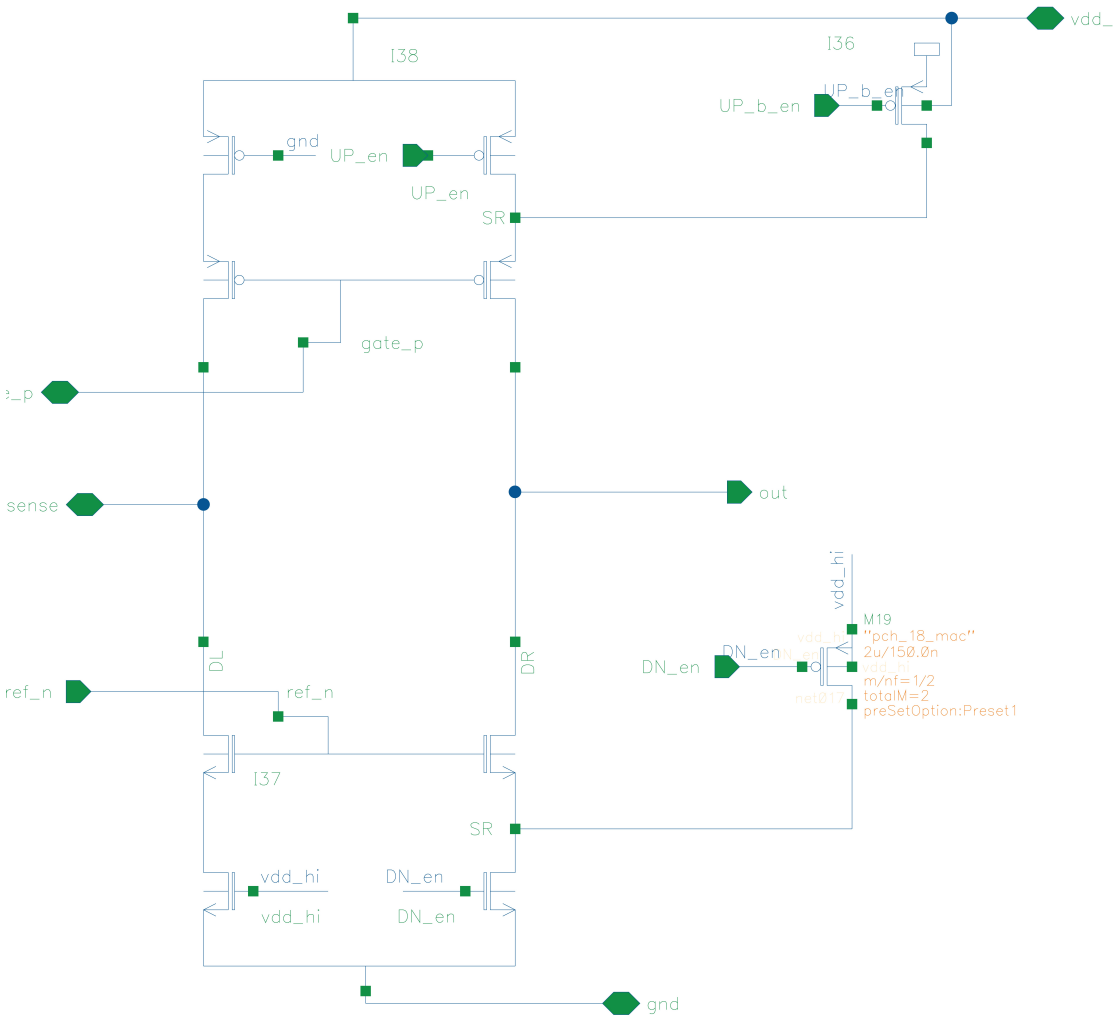
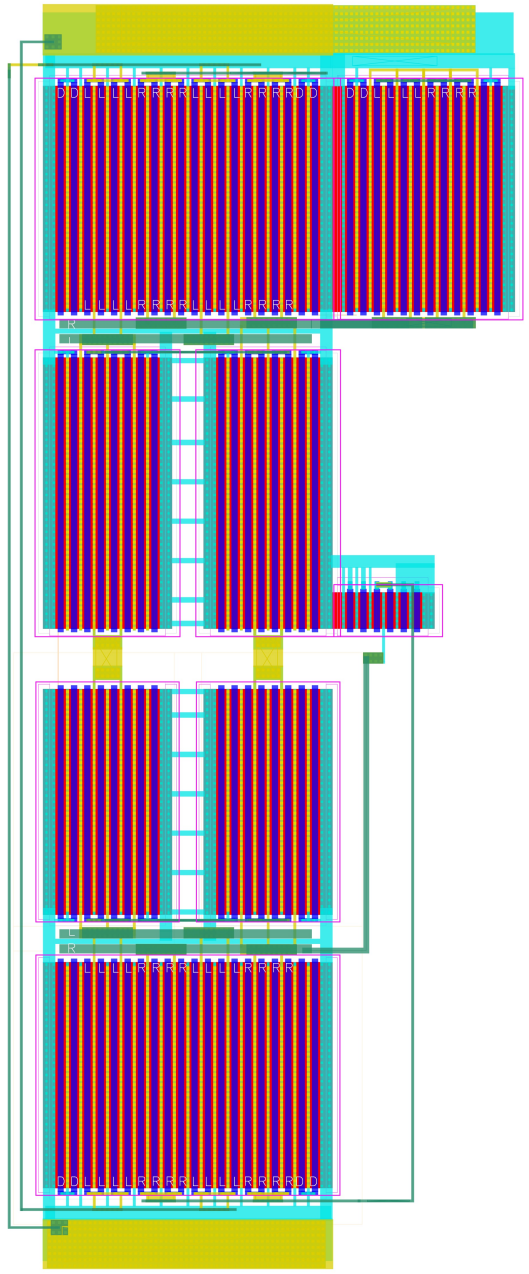
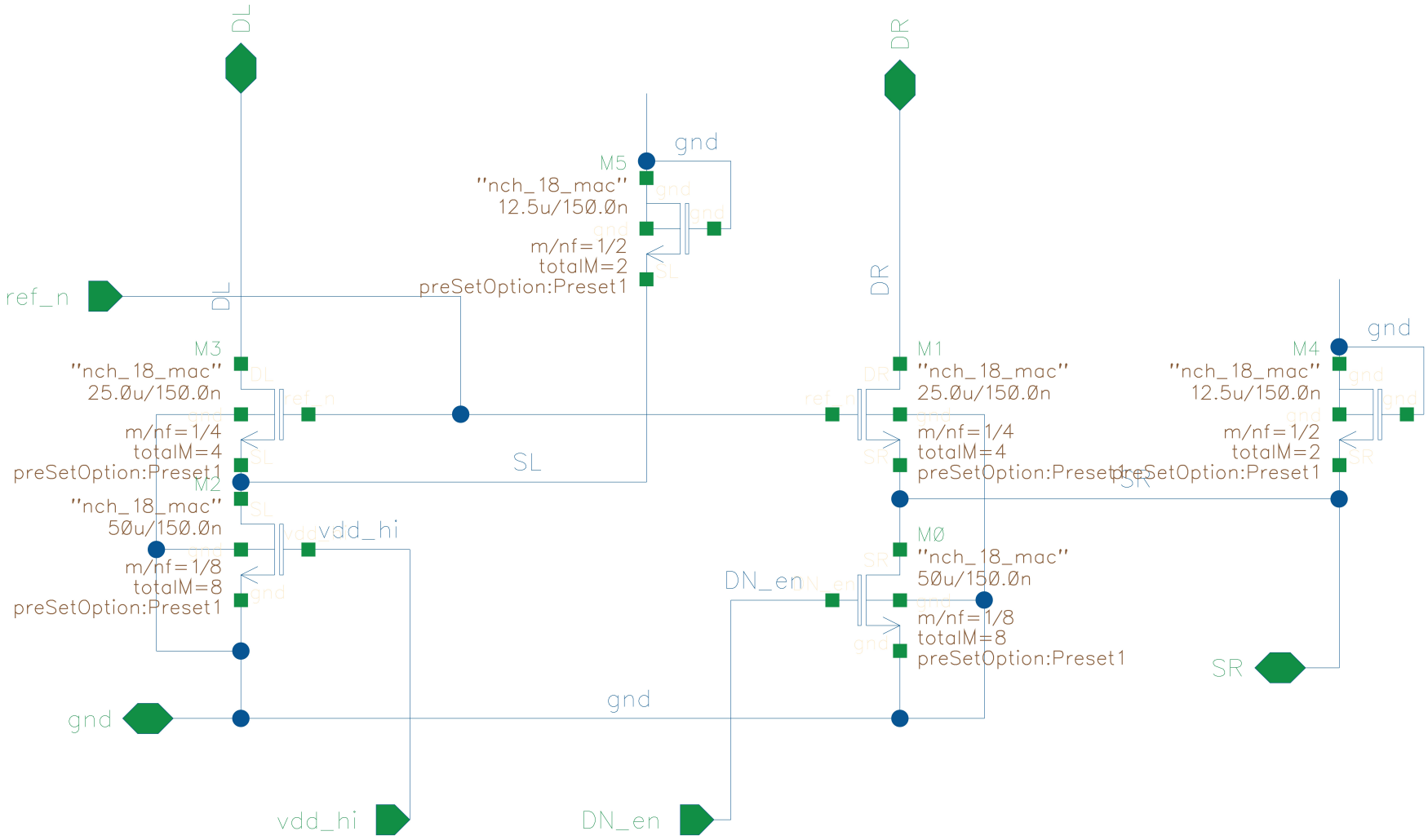
Layout Example: Charge Pump

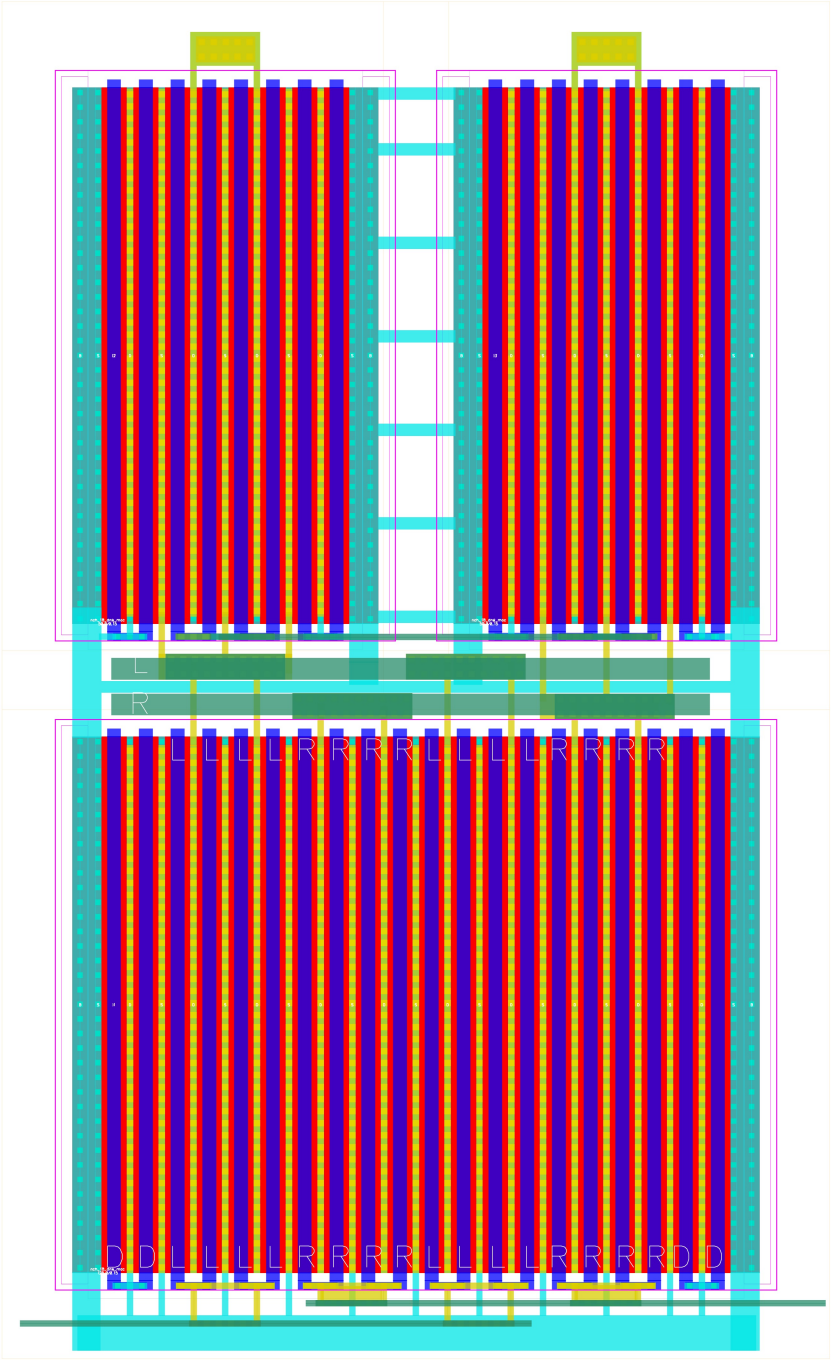




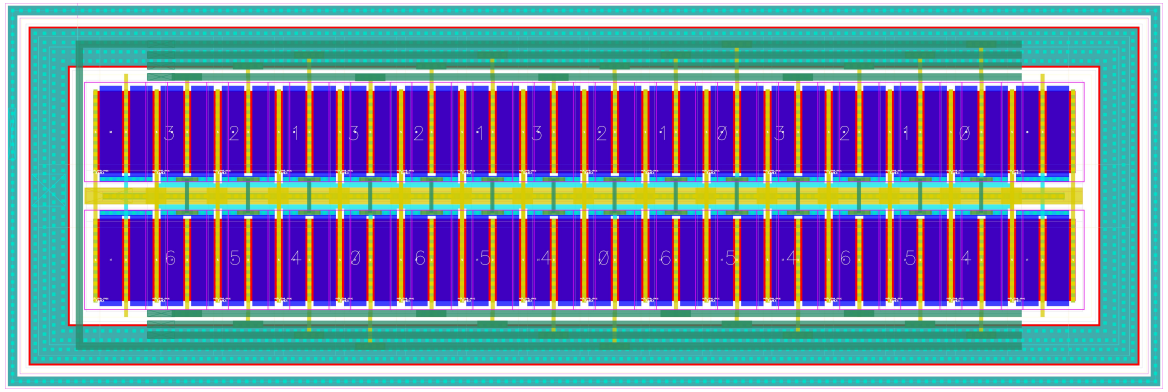
Charge Pump: N-Mirror



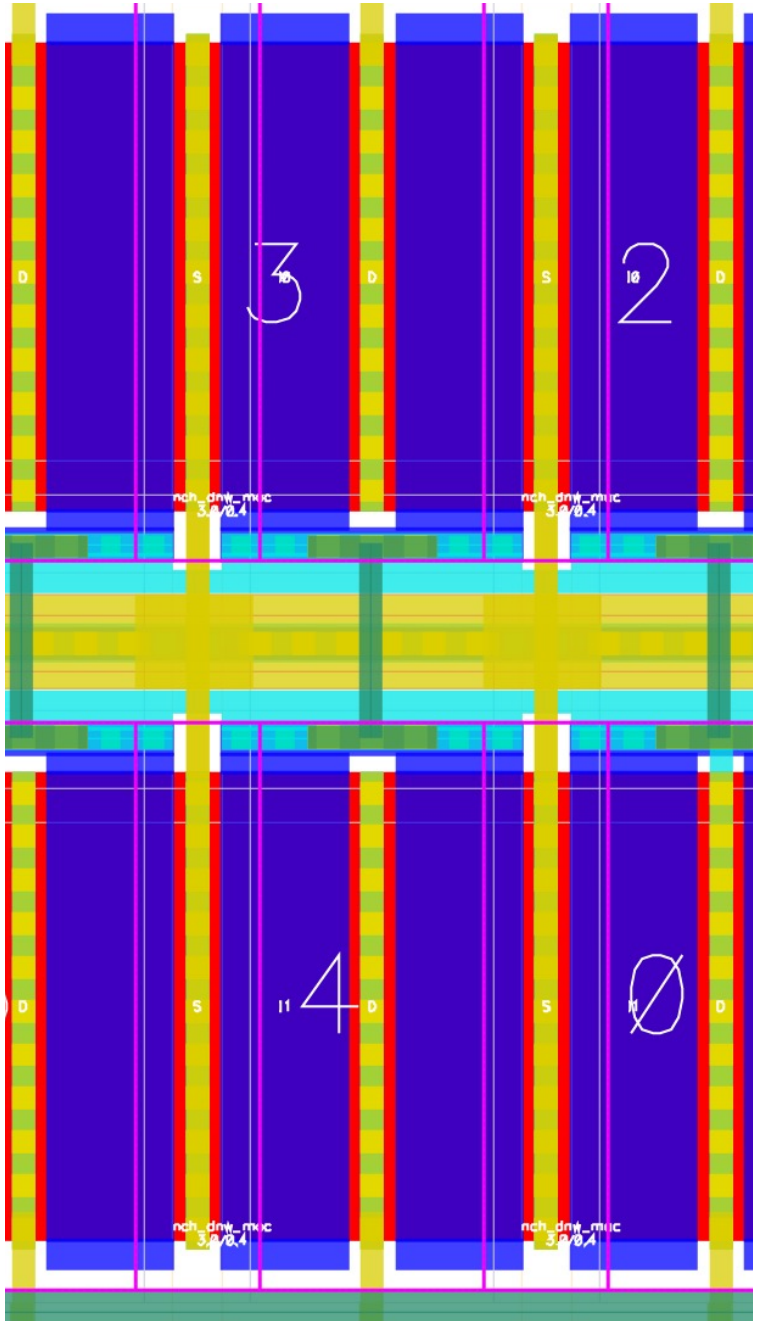
N-Mirror Layout



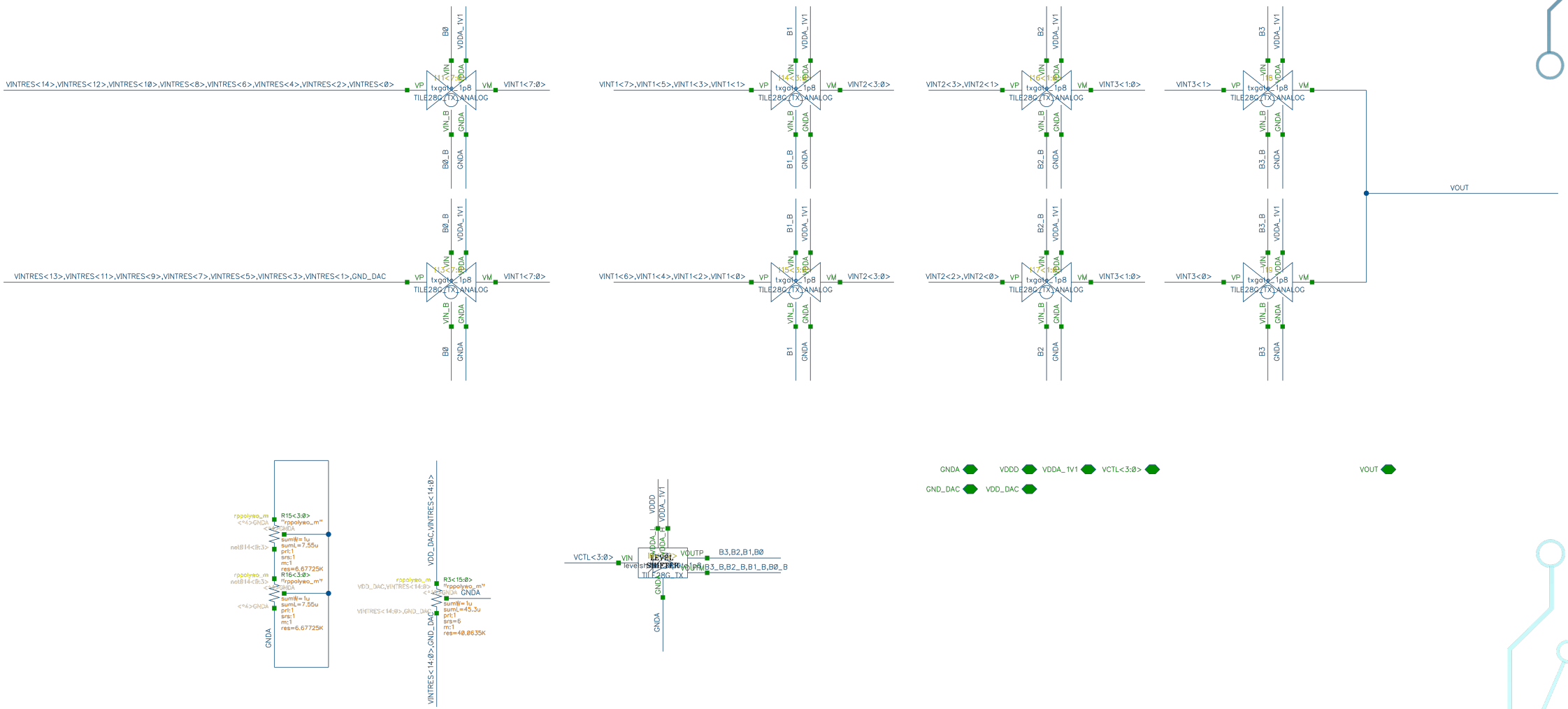
Make a “Unit Cell”



- In analog layout, the best results (not the most area efficient) are obtained by using a “unit cell” and replicating the unit cell
- Make the “environment” around the cell as matched as possible

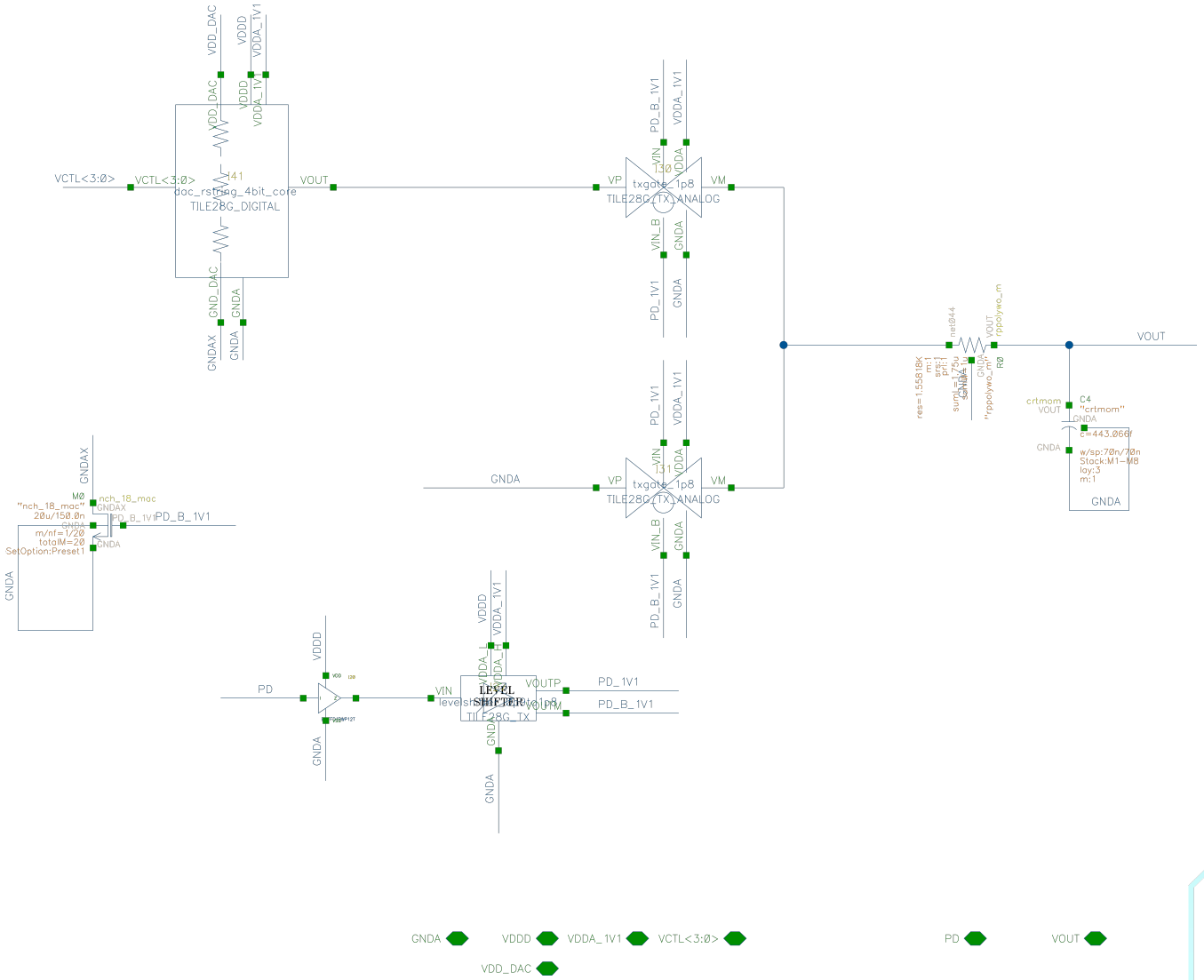


Example: R-DAC Design

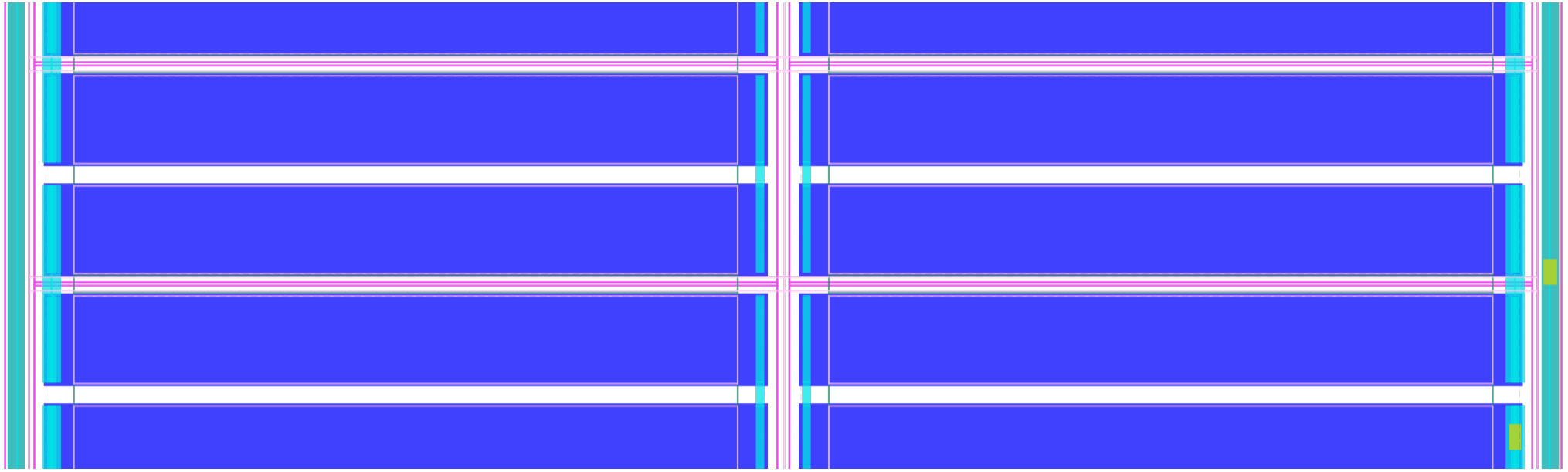


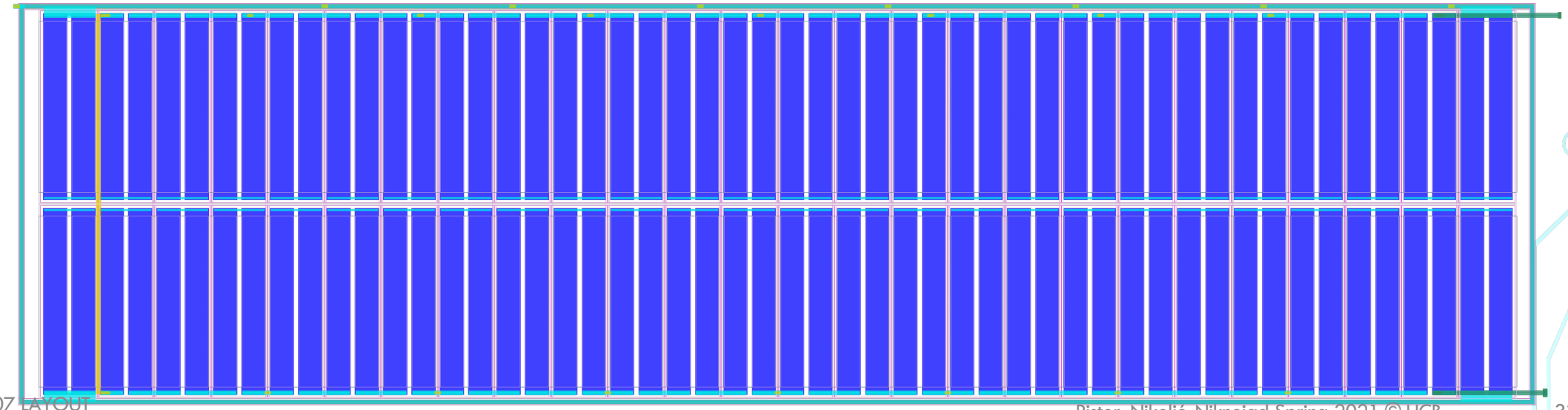
Aside on Good Design Practices

- Make an enable and make sure current is zero when “off”
- Make a default value of zero or vdd when off
- Put a filter on the output of this DAC (good practice since it’s a DC)
- Make sure you don’t drive any loads except gates since there’s no output buffer

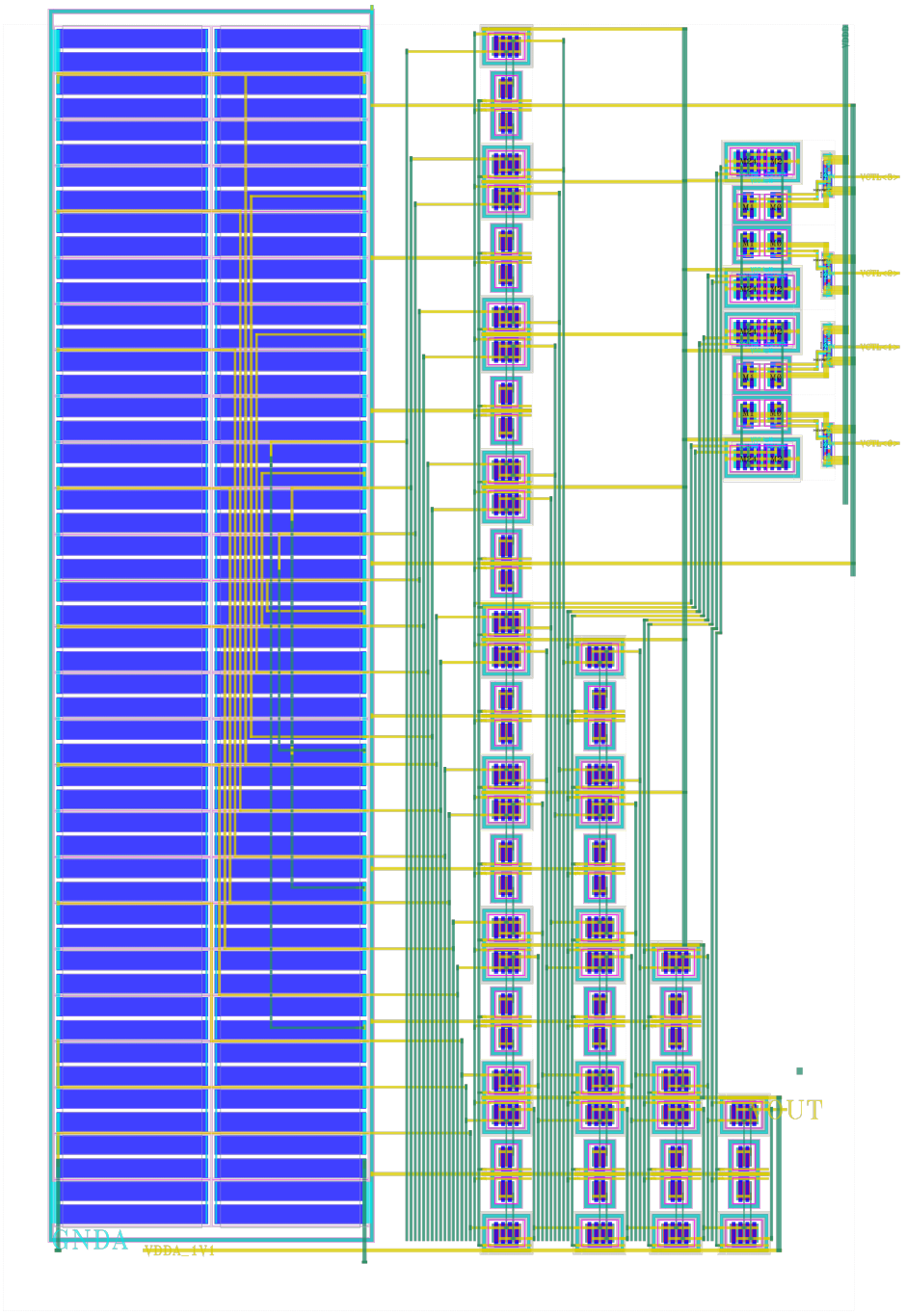


Layout – Unit Cell Concept

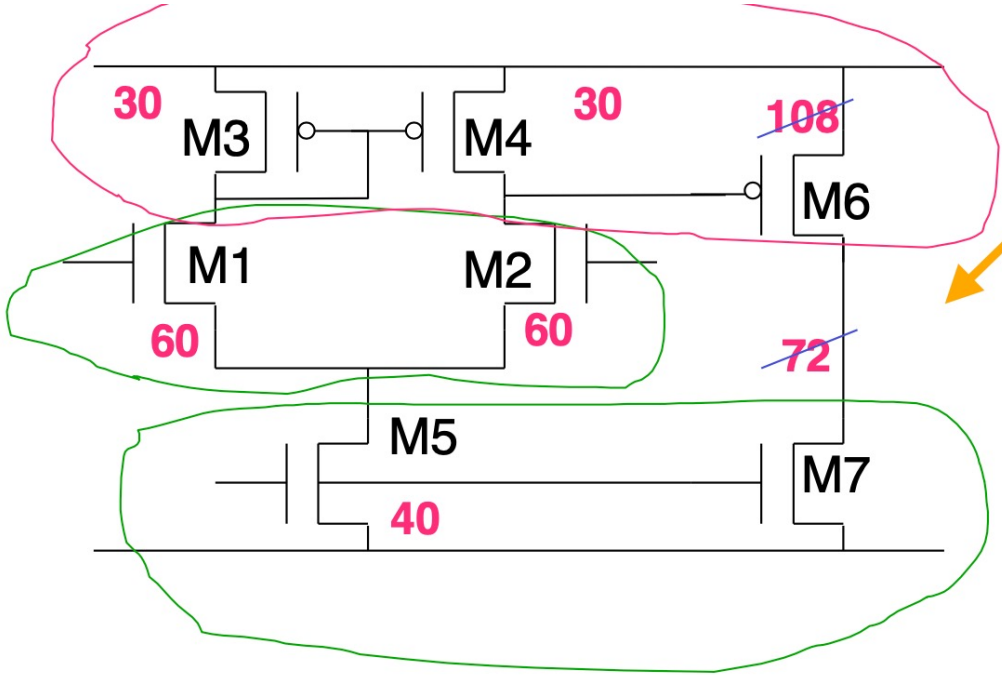


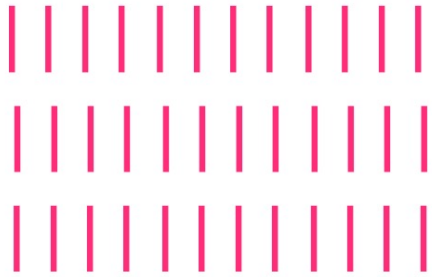


Top Level



Example: OTA Layout





M3, M4, M6

M1, M2

M5, M7

Only width matters

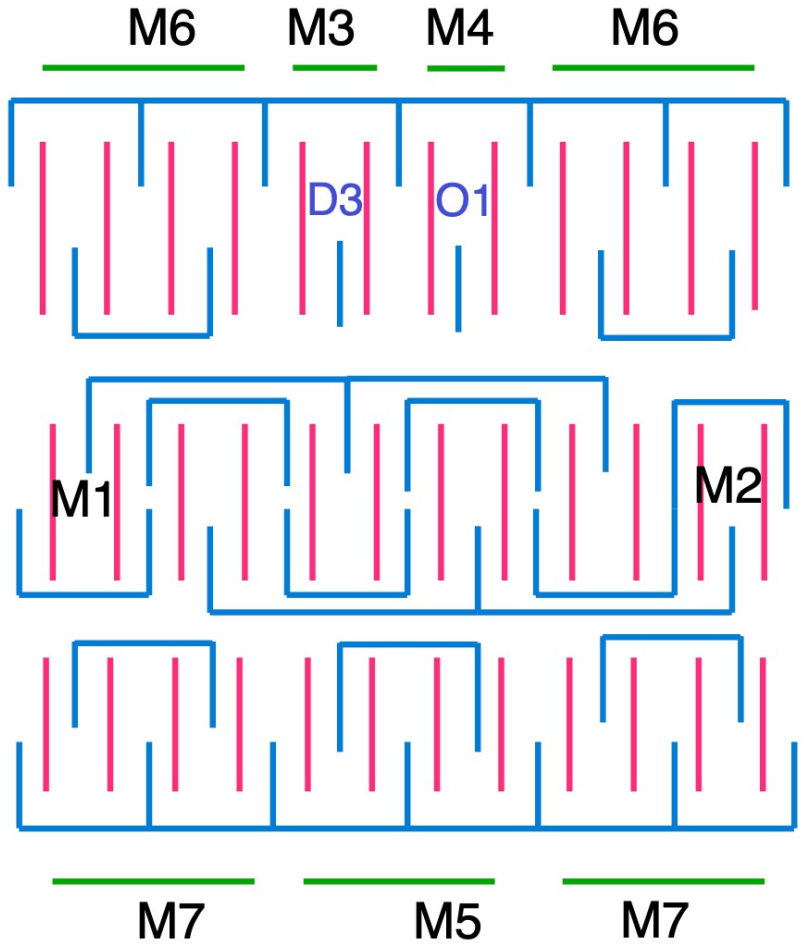
Possible stacks:
1 p-channel, 2 n-channel

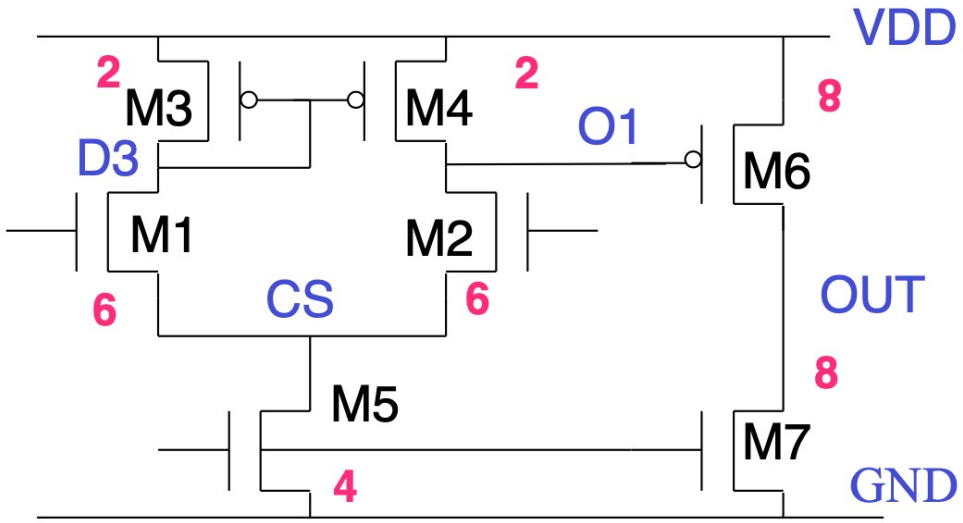
change the size of M6 and M7 to 80 and 120 respectively

Width of each finger?
We want the same number of fingers per stack (k).
W_{p1} = 180/k
W_{n1}=120/k
W_{n2}=120/k

for M3 and M4 use 2 fingers

OTA Layout Continued

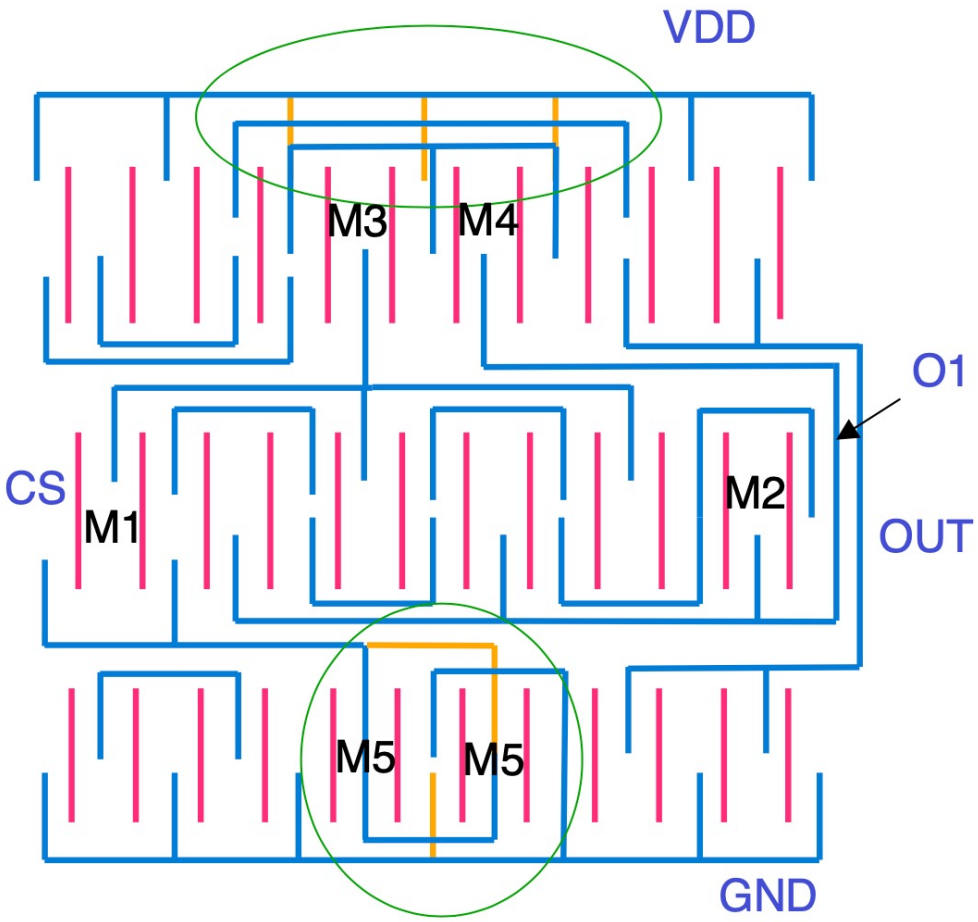


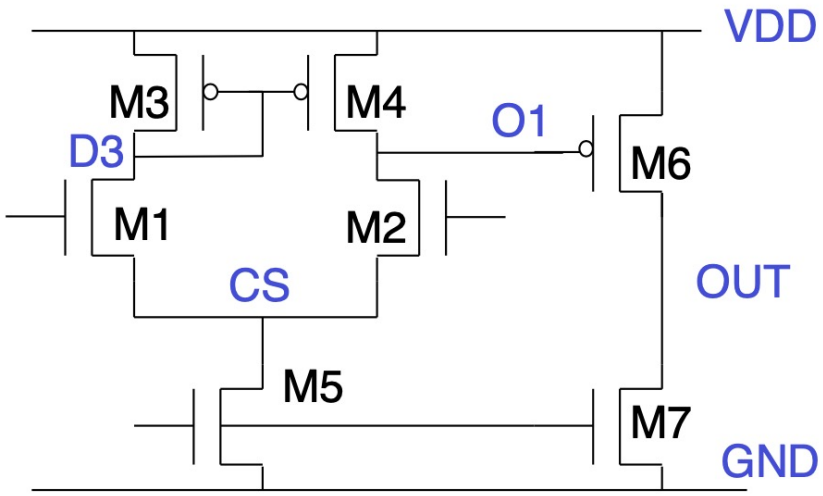


First attempt of interconnections (not completed)

Maloberti, F, "Layout of Analog CMOS Integrated Circuits" (Part 2)

Metal Interconnect





Use metal for carrying current!
Poly connections are not a problem (usually)

Layout of Passives

Process Options

- Available for many processes
- Add features to “baseline process”
- E.g.
  - Capacitor option (MIM, 2 level poly, channel implant)
    - Note that “MOM” capacitors are free (no extra layers)
  - Low V_{TH} devices
  - “High voltage” devices (3.3V) [Always have thick oxide IO devices)
  - Flash
  - Silicide stop option
  - …

Passives: Resistors

- No provisions in standard CMOS
- Resistors are bad for digital circuits →
  - Minimized in standard CMOS
- Sheet resistance of available layers:

Layer	Sheet resistance
Aluminum	60 mΩ/□
Polysilicon	5 Ω/□
N+/P+ diffusion	5 Ω/□
N-well	1 kΩ/□

- Example: 100kΩ poly resistor
  → 1μm wide by 20,000μm long

Silicide Technology

- Implants used to lower resistance of source/drain and polysilicon.
- Titanium Silicide ($TiSi_2$) is widely used salicide (self-aligned silicide), has low resistivity (13-17 $m\Omega$-cm) with melting point of 1540°C. Another widely used silicide is $CoSi_2$.
- Platinum Silicide (PtSi) is a highly reliable contact metallization between the silicon substrate and the metal layers (Al).

Silicide Block Option

Layer	R/□ [Ω/□]	T_C [ppm/°C] @ T = 25 °C	V_C [ppm/V]	B_C [ppm/V]
N+ poly	100	-800	50	50
P+ poly	180	200	50	50
N+ diffusion	50	1500	500	-500
P+ diffusion	100	1600	500	-500
N-well	1000	-1500	20,000	30,000

- Non-silicided layers have significantly larger sheet resistance
- Resistor nonidealities:
  - Temperature coefficient: R = f(T)
  - Voltage coefficient: R = f(V)

Resistor Example

Goal: R = 100 kΩ, $T_C = 1/R \times dR/dT = 0$

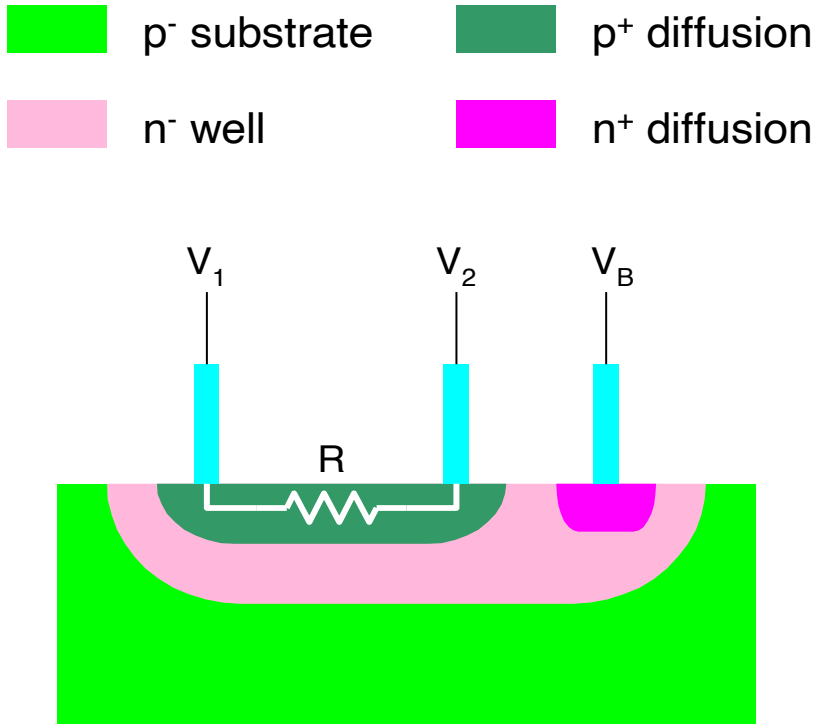
Solution: combination of N+ and P+ poly resistors in series

$$R = R_N(1 + T_{CN}\Delta T) + R_P(1 + T_{CP}\Delta T)$$
$$= \underbrace{R_N + R_P}_{R} + \underbrace{(R_N T_{CN} + R_P T_{CP})}_{0}\Delta T \quad \Rightarrow$$

$$R_N = R\frac{1}{1 - \frac{T_{CN}}{T_{CP}}} = 20\text{k}\Omega = 200 \text{ squares}$$

$$R_P = R\frac{1}{1 - \frac{T_{CP}}{T_{CN}}} = 80\text{k}\Omega = 444.4 \text{ squares}$$

Voltage Coefficient



Example:
Diffusion resistor

→ Applied voltage modulates depletion width
(cross-section of conductive channel)

→ Well acts as a shield

$$R = \frac{V_1 - V_2}{I}$$

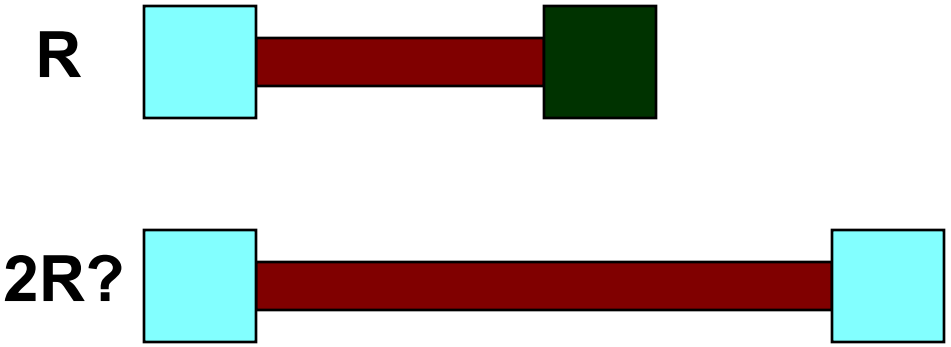
$$\approx R_o\left[1 + T_C\left(T - 25^o\right) + V_C\left(V_1 - V_2\right) + B_C\left(\frac{V_1 + V_2}{2} - V_B\right)\right]$$

Resistor Matching

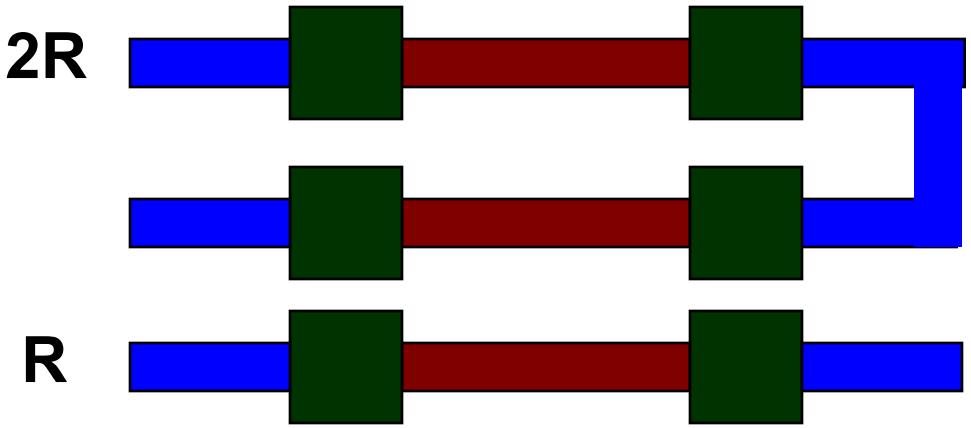
- Types of mismatch
  - Systematic (e.g. contacts)
  - Run-to-run variations
  - Random variations between devices
- Absolute resistor value
  - E.g. filter time constant, bias current (BG reference)
  - ~ 15 percent variations (or more)
- Resistor ratios
  - E.g. opamp feedback network
  - Insensitive to absolute resistor value
  - “unit-element” approach rejects systematic variations (large area for non-integer ratios)
  - Process gradients
  - 0.1 … 1 percent matching possible with careful layout

Systematic Variations from Layout

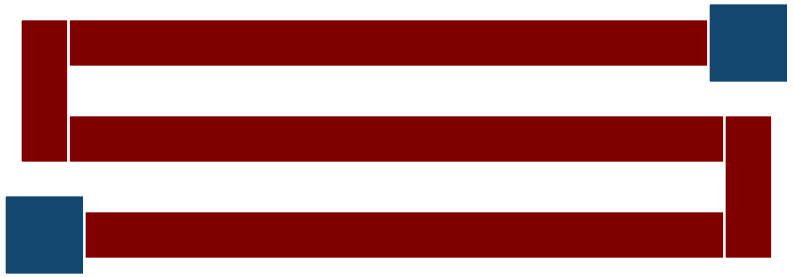
- Example:



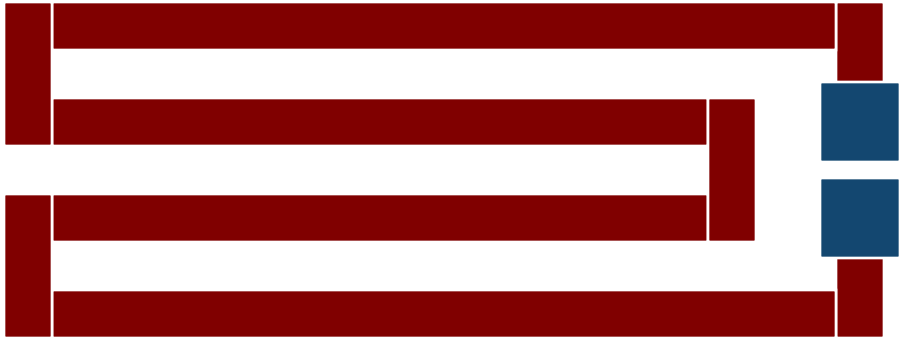
- Use unit element instead:



Serpentine layout for large values:

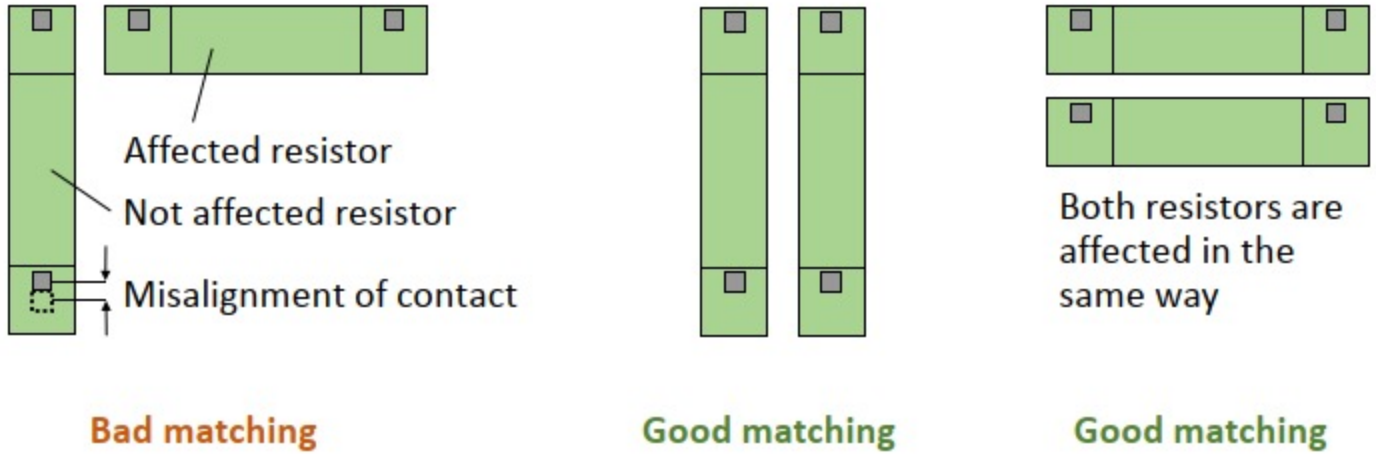


Better layout (mitigates offset due to thermoelectric effects):



See Hastings, “The art of analog layout,” Prentice Hall, 2001.

Misalignment



Electromigration and Parasitics

- **Electromigration rules limit maximum current density**
  - Same value resistance must be physically larger to carry more current
  - Hence, more current → larger capacitive parasitcs

Capacitors

- Simplest capacitor:

substrate

- **What's the problem with this?**

Capacitors

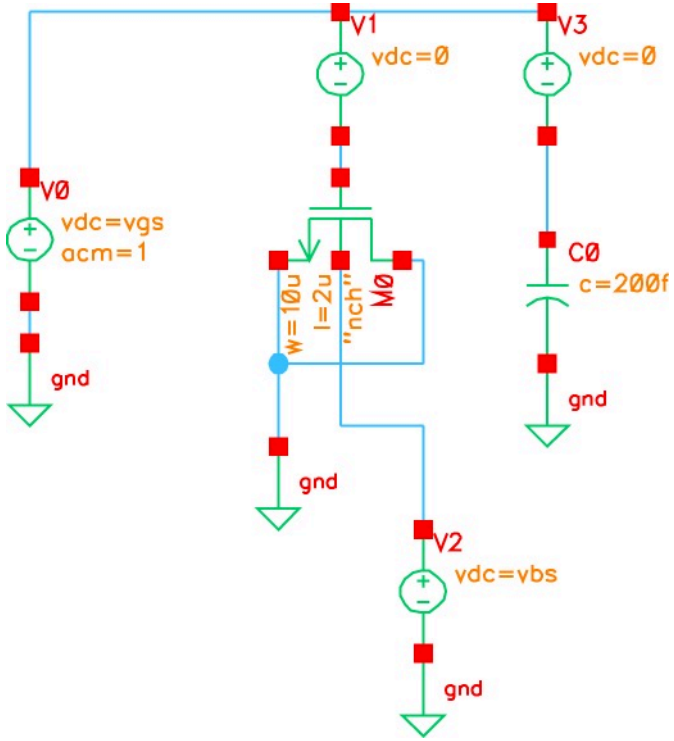
- "Improved" capacitor:

- **Is this only 1 capacitor?**

Capacitors Options

Type	C [aF/μm^2]	V_C [ppm/V]	T_C [ppm/^{o}C]
Gate (thick oxide)	8000	Huge	Big
MIM (option)	4000		
MOM (> 5 metals)	~2000		
Poly-poly (option)	1000	10	25
Metal-metal	50	20	30
Metal-substrate	30		
Metal-poly	50		
Poly-substrate	120		
Junction capacitors	~ 1000	Big	Big

MOS Capacitor



- High capacitance in inversion:
  - Linear region
  - Strong inversion
- SPICE:

$$C = \frac{I}{\omega V}$$

$$V = 1V$$

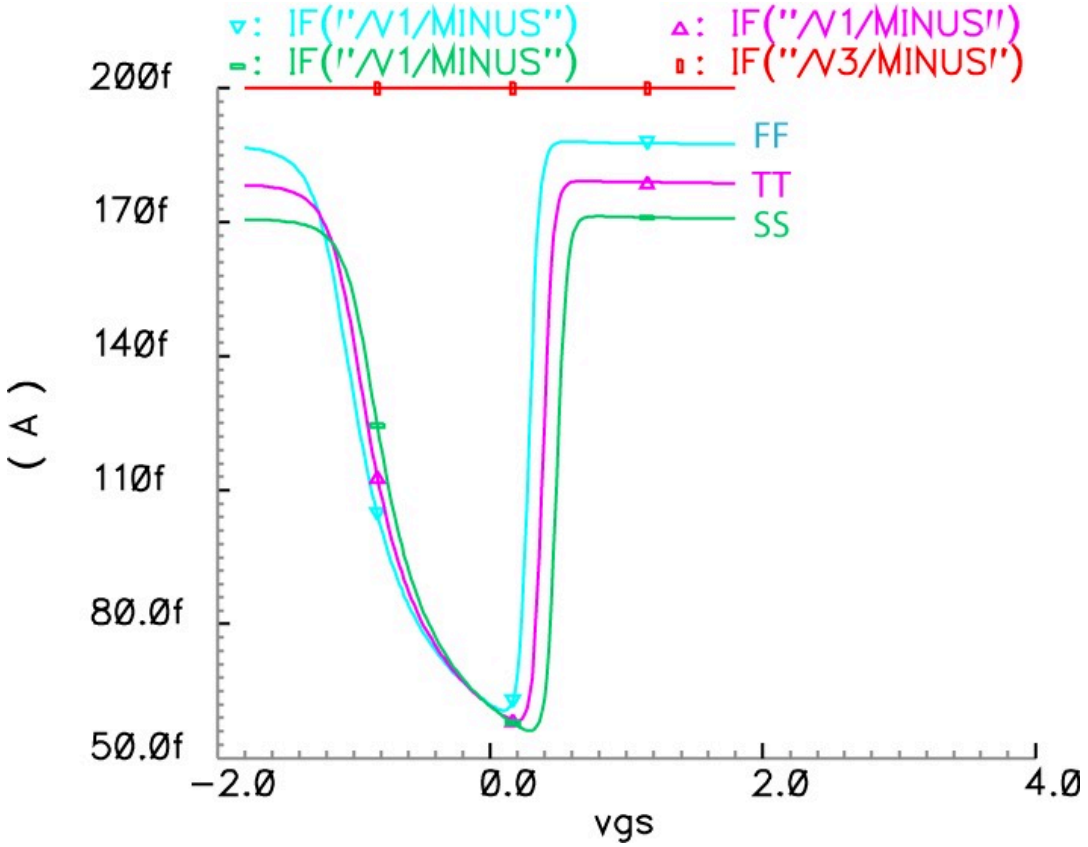
$$\omega = 1$$

$$\rightarrow C = I$$

MOS Capacitor

- High non-linearity, temperature coefficient

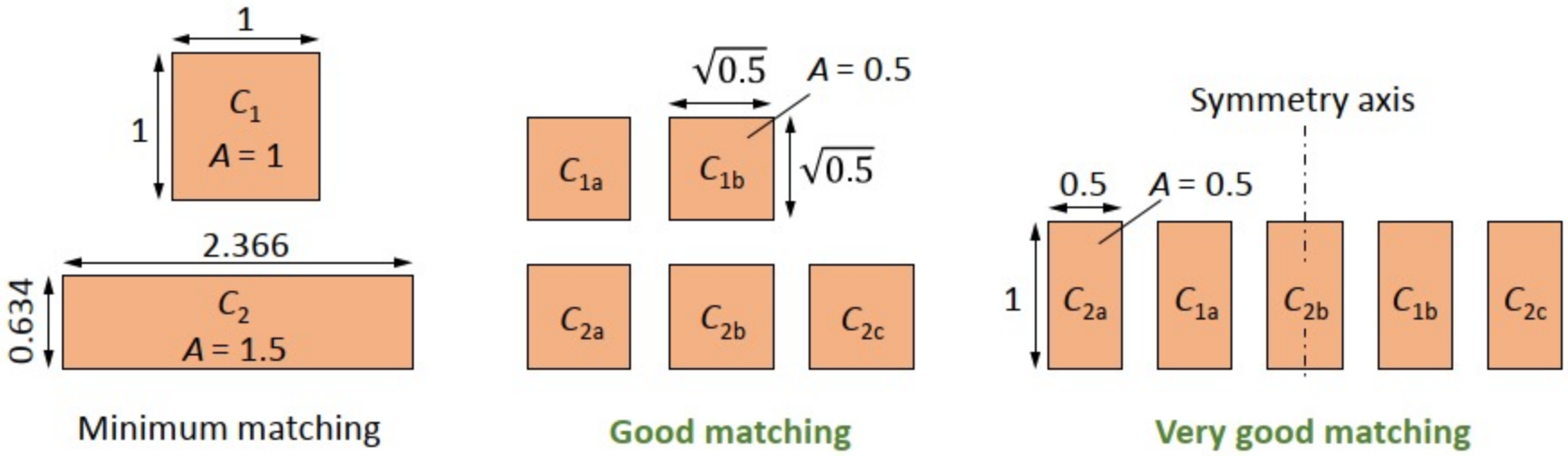
- But, still useful in many applications, e.g.:
  - (Miller) compensation capacitor
  - Bypass capacitor (supply, bias)



Poly-Poly Capacitor

- Applications:
  - Feedback networks
  - Filters (SC and continuous time)
  - Charge redistribution DACs & ADCs
- Cross-section
- Bottom- and top-plate parasitics
- Shields

Matching Capacitors



Excellent matching…

Capacitor Layout

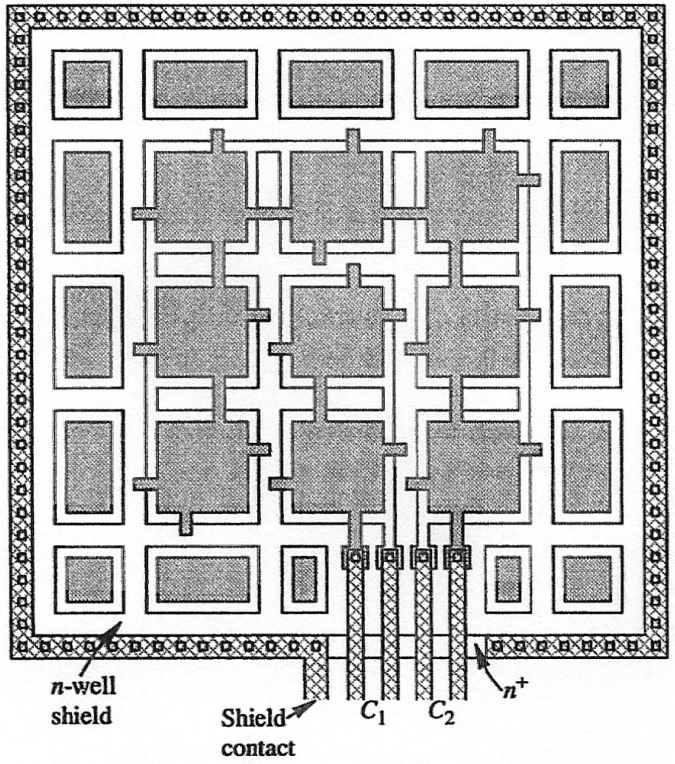


Figure 6.17 A layout of two capacitors with ratio $C_2/C_1 =$ ½, incorporating several of the techniques discussed in the text (adapted from Ref. 23).

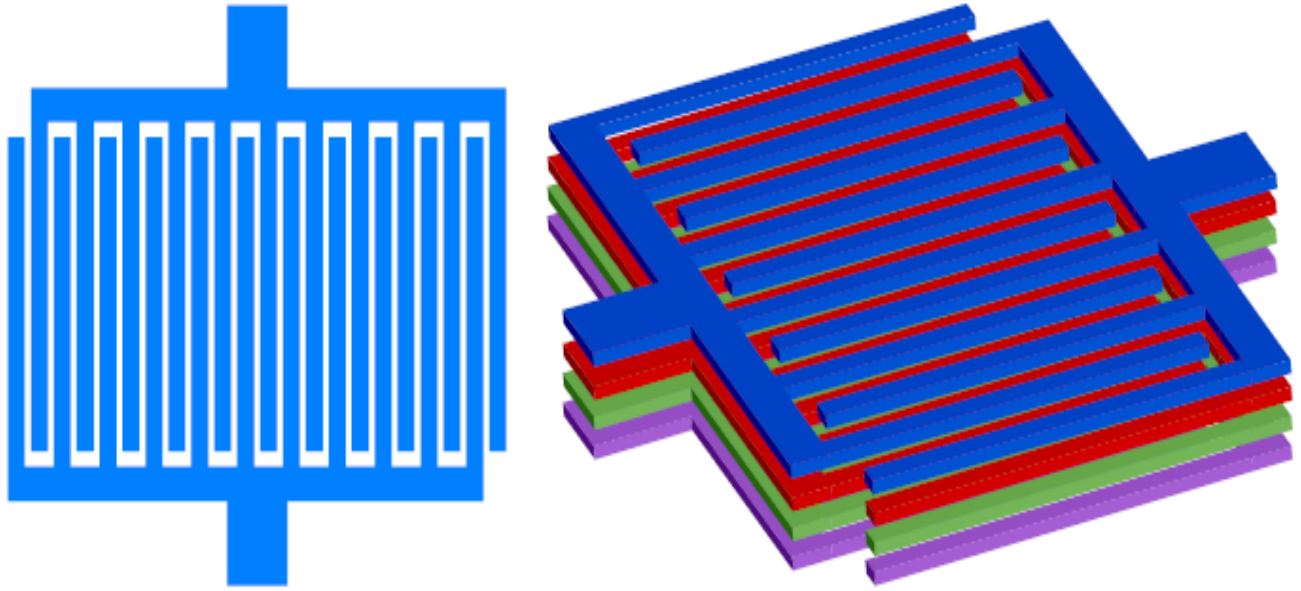
- Unit elements
- Shields:
  - Etching
  - Fringing fields
- "Common-centroid"
- Wiring and interconnect parasitics

Ref.: Y. Tsividis, "Mixed Analog-Digital VLSI Design and Technology," McGraw-Hill, 1996.

MIM Capacitors

- Many processes have add-on options such as a MIM capacitor.
- This is simply a metal-insulator-metal (MIM) structure situated in the oxide layers. The insulator is a very thin layer (~25 nm), resulting in high density and relatively low back-plate parasitics.

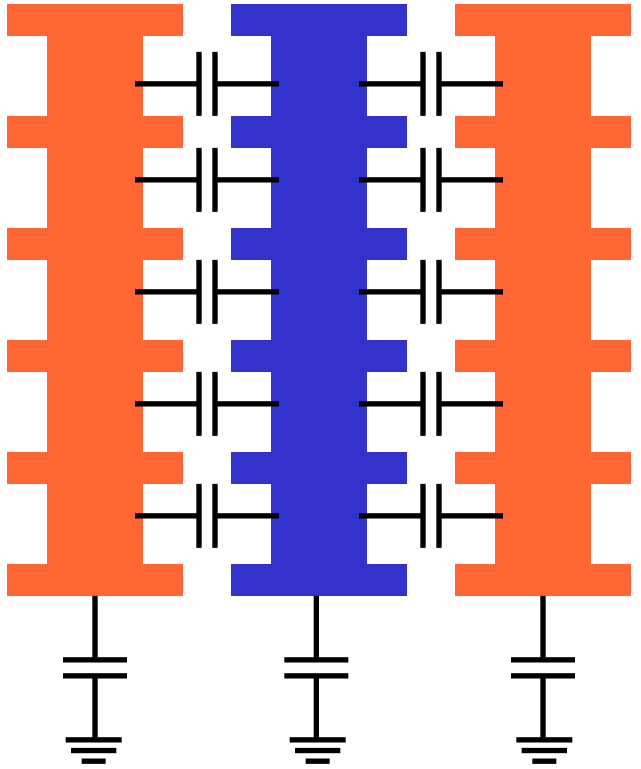
“MOM” Capacitors



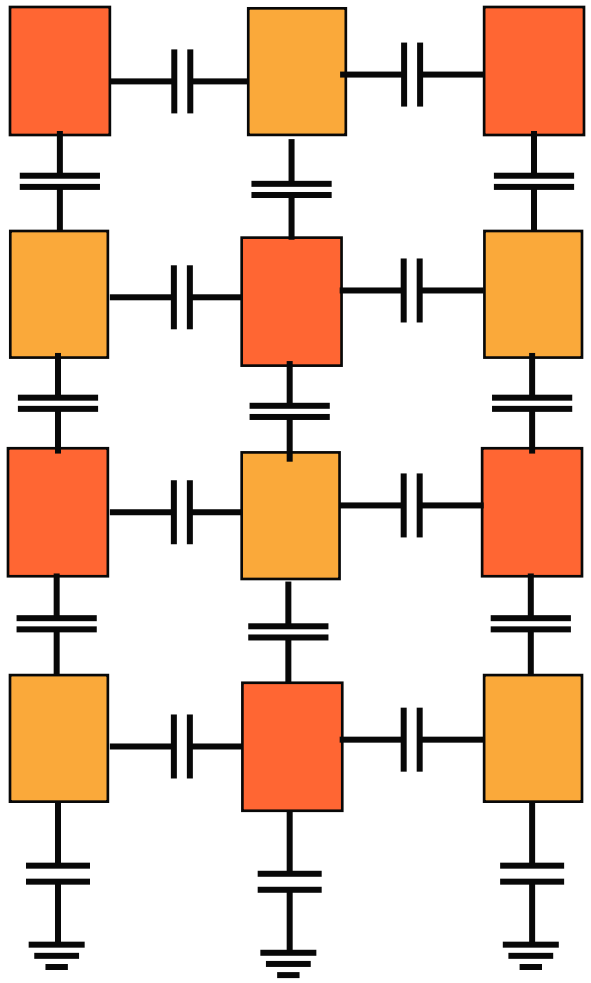
- Metal-Oxide-Metal capacitor. Free and most common in modern CMOS.
- Use lateral flux (~L_{min}) and multiple metal layers to realize high capacitance values

MOM Capacitor Cross Section

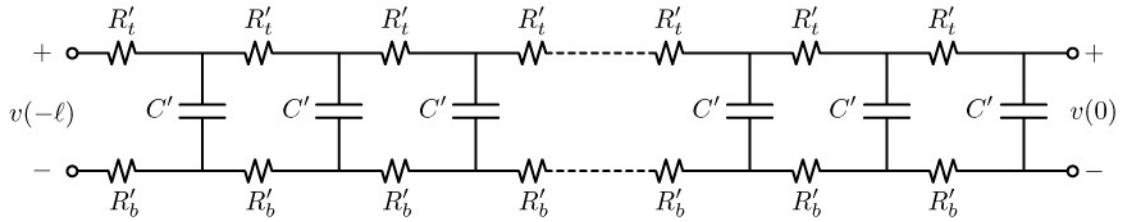
- Use a wall of metal and vias to realize high density
- More layers – higher density
  - May want to chop off lower layers to reduce C_{bot}
- Reasonably good matching and accuracy

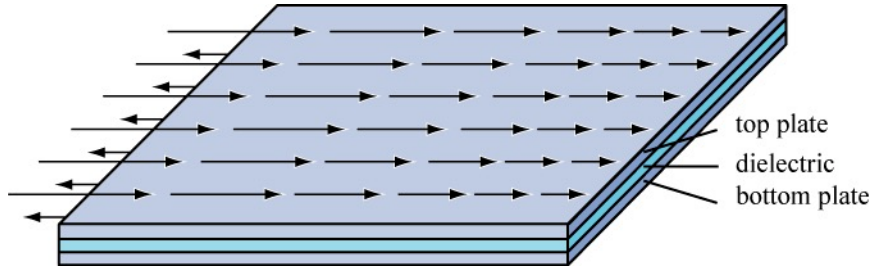


Another MOM Option



Capacitor Q





- Current density in capacitor plates drops due to vertical displacement current.
- Must analyze the distributed RC circuit…

Capacitor Impedance

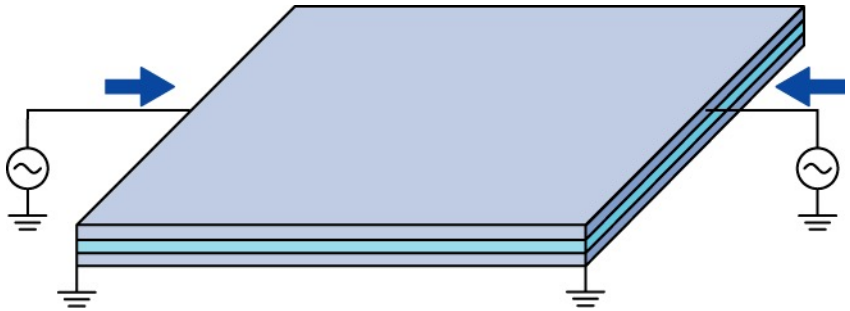
- For a capacitor contacted at one side, we can show that

$$Z_{in} = \frac{\gamma}{j\omega C'} \coth(\gamma \ell)$$

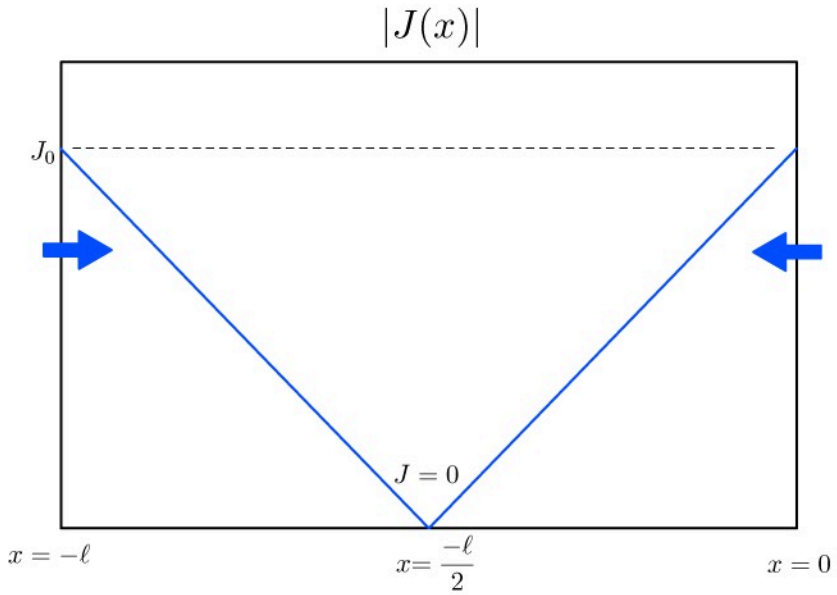
- We can simplify this for small structures

$$Z_{in} \approx \frac{R_T + R_B}{3} + \frac{1}{j\omega C}$$

Double Contact Strucutre

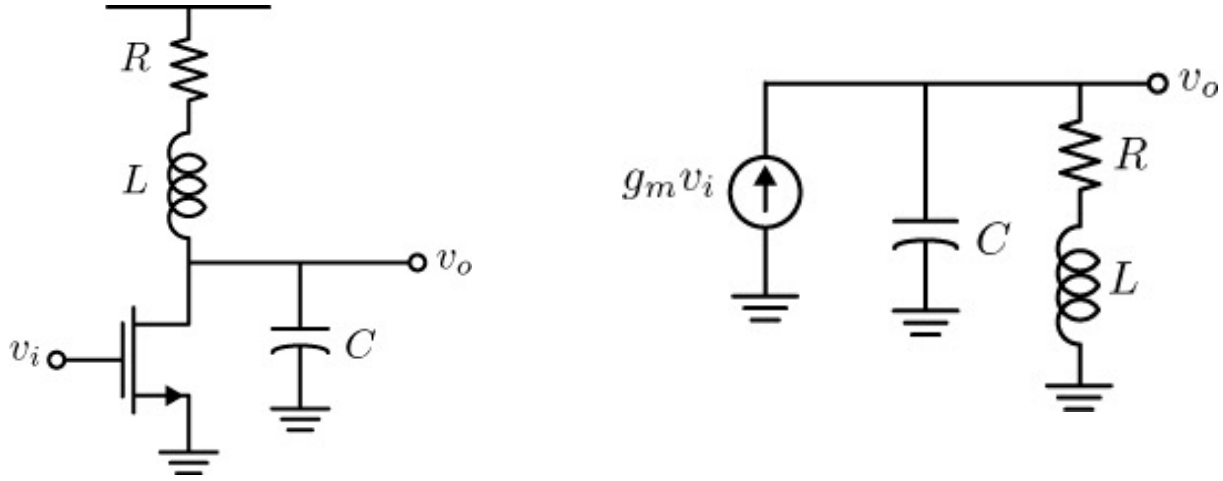


$$Z_{in} \approx \frac{R}{12} + \frac{1}{j\omega C}$$



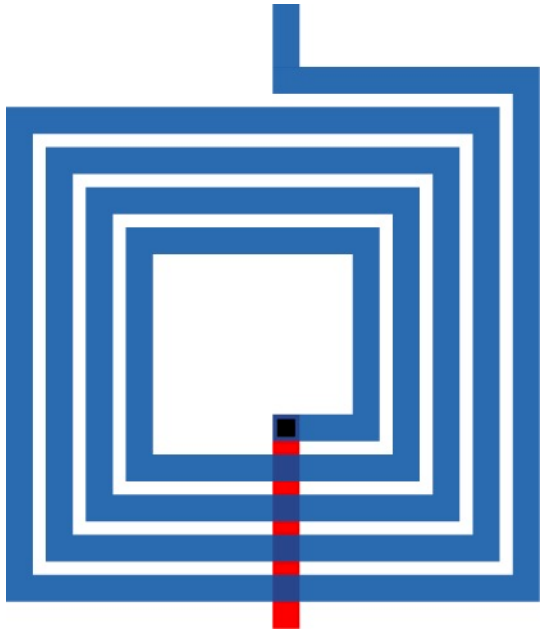
- Instead of doing distributed analysis, we can guess the current distribution as linear and quickly calculate the effective resistance.
- For a double contact case, the resistance drops by 4 times.

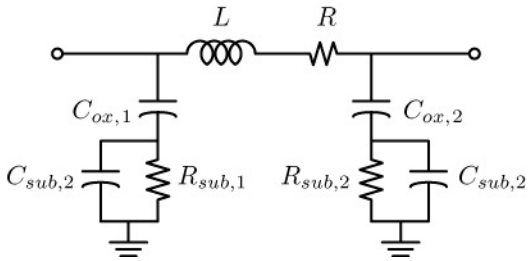
What About Inductors?

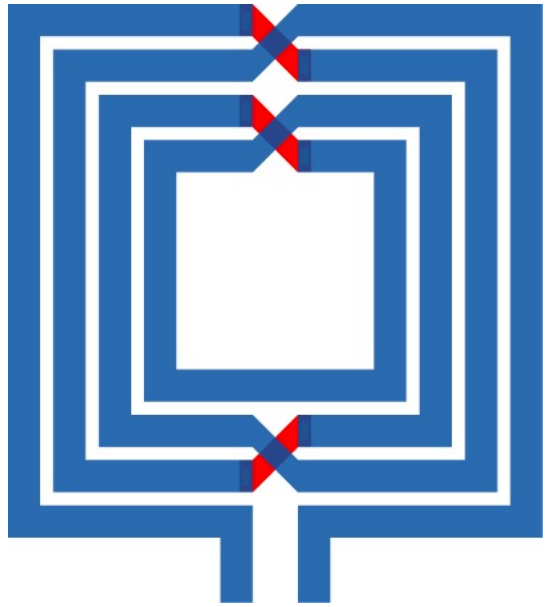


- Mostly not used in analog/mixed-signal design
  - Usually too big
  - More of a pain to model than R's and C's
  - But they do occasionally get used
- Example inductor app.: shunt peaking
  - Can boost bandwidth by up to 85%!
  - Q not that important (L in series with R)
  - But frequency response may not be flat

Spiral Inductors

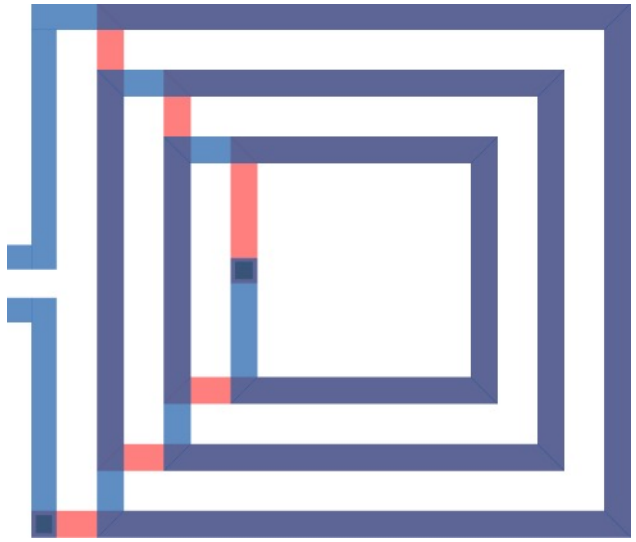




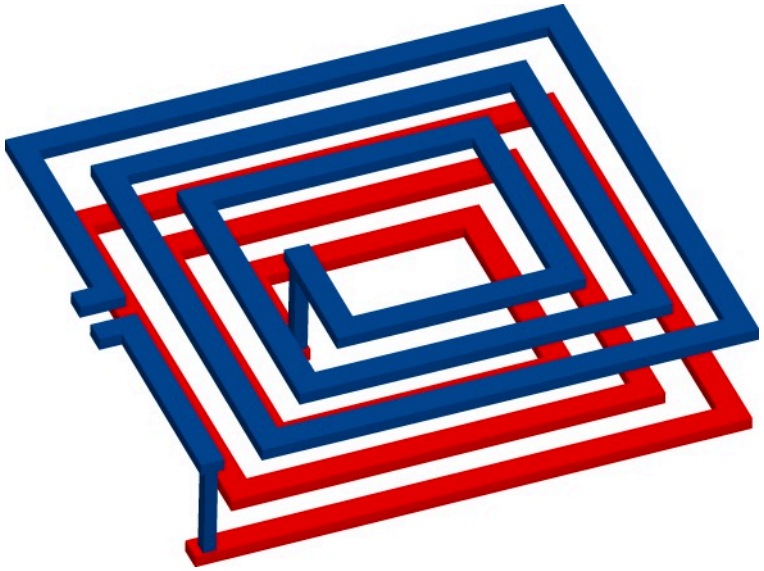


- Used widely in RF circuits for small L (~1-10nH).
- Use top metal for Q and high self resonance frequencies.
  - Very good matching and accuracy – if you model them right

Multi-Layer Inductors



Top view



3D view (not to scale)

- By taking advantage of multiple metal layers and mutual coupling, we can realize very large inductors (~ 100 nH).

References

- Lienig, Scheible, "Fundamentals of Layout Design for Electronic Circuits," Springer 2020.
- Maloberti, F, "Layout of Analog CMOS Integrated Circuits" (Part 2)
- Hastings, "The art of analog layout," Prentice Hall, 2001.
- A. M. Niknejad, *Electromagnetics for High-Speed Analog and Digital Communication Circuits*, Cambridge University Press, 2007. (pdf)

Layout Editing Concepts

- Polygons
  - Merge
  - Chop
- F4 → options
- Array Copy vs Tile
- Vias
- Stretching / Edges
- Live DRC / DRD editing
- MPP's (Multi-Part Path)
- Grouping vs Hierarchy
  - Edit in place
- Bus layout

- Learn to Probe Nets / Mark Nets
- Learn how to do a hierarchy copy (and modify cells to point to new cells)