EE290C: 28nm SoC for IoT

The Layout Lecture

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- Please do not post these slides on the Internet. There are no “secrets” in these slides, but they contain some actual layouts from my consulting.

Topics

Part 1

- Layout of a FET 3T
  - Dimensions, fingers, dummy
  - DFM
- PMOS vs NMOS
- Body contacts 4T
- DNW and 5T and 6T transistors

Part 2

- Analog Layout
  - Matching
  - Common centroid
  - Symmetry
  - Unit Cell Concept
- Current Source
- Differential Pair

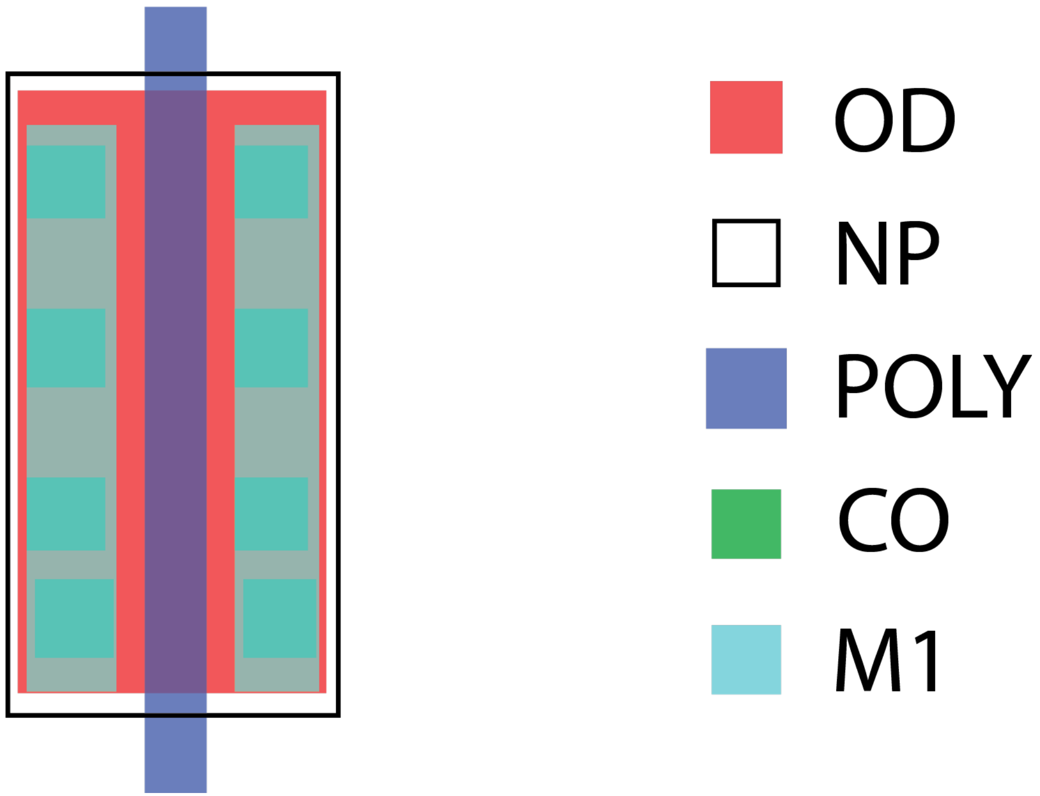
Part 3

- Capacitors
  - Love your MOM
- Resistors
- More arrays
- Inductors
- Electromigration Rules
- Antenna Rules
- Examples:
  - DAC
  - Op-Amp
  - Tiles of blocks
  - Pin placement
- Layout Hierarchy vs Schematic

Transistors

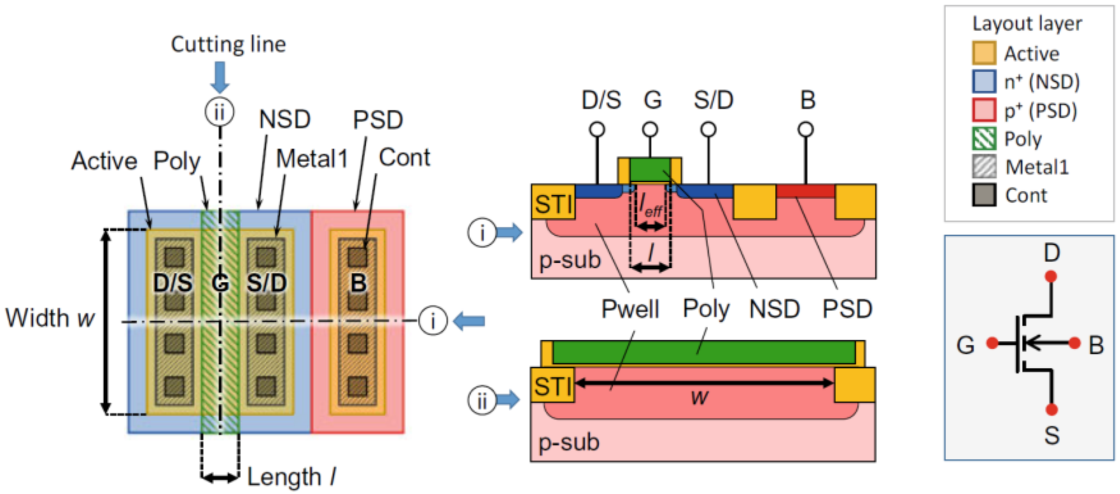
3T FET

- From schematic, it's W and L and maybe threshold flavor
- What about NF
- Layout Layers / Cross Section
  - OD
  - NP (PP)
  - POLY
  - M1
  - CO

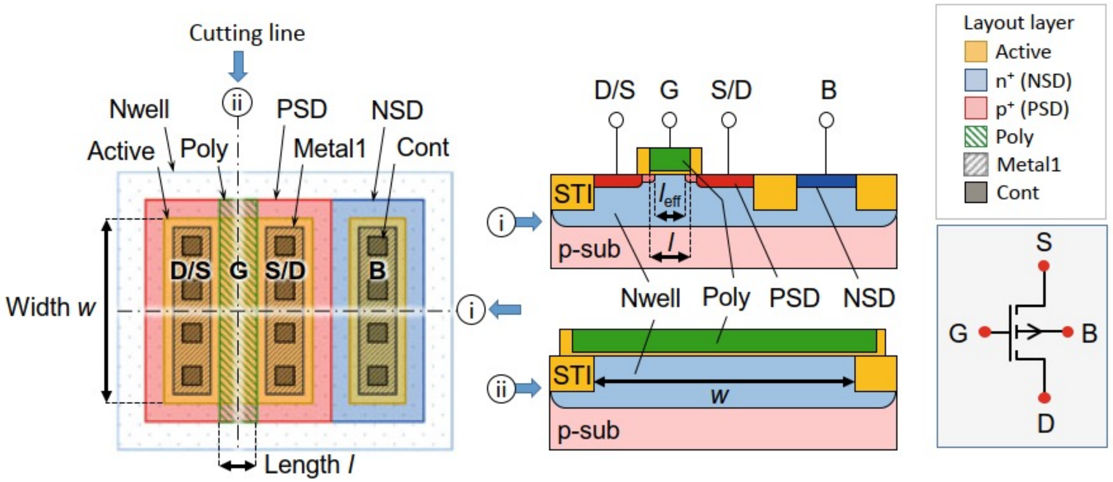


Transistor Layouts

- NMOS



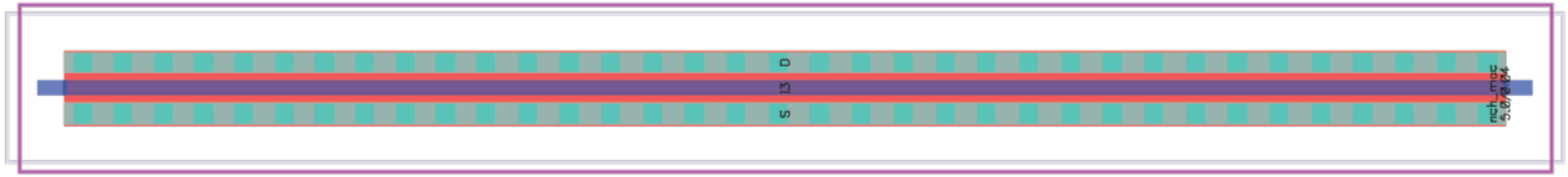
- PMOS

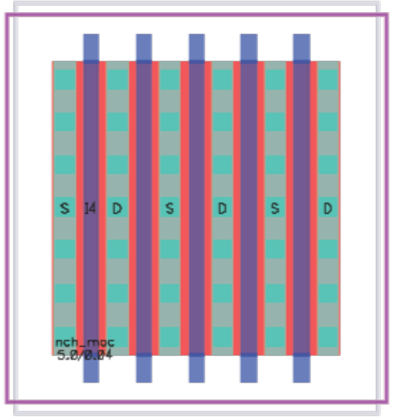


Lienig, Scheible, “Fundamentals of Layout Design for Electronic Circuits,” Springer 2020.

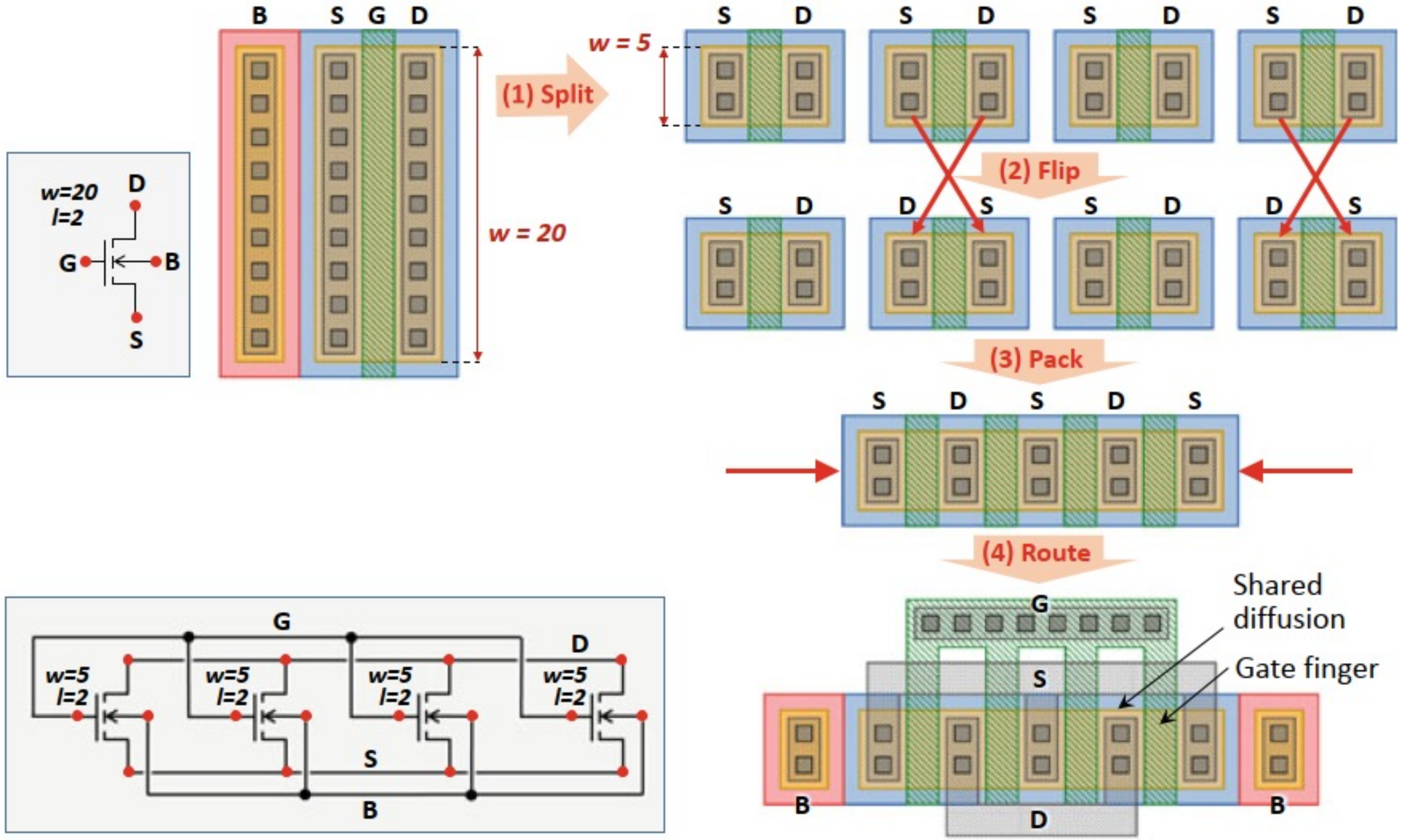
Fingers

- Why use fingers?





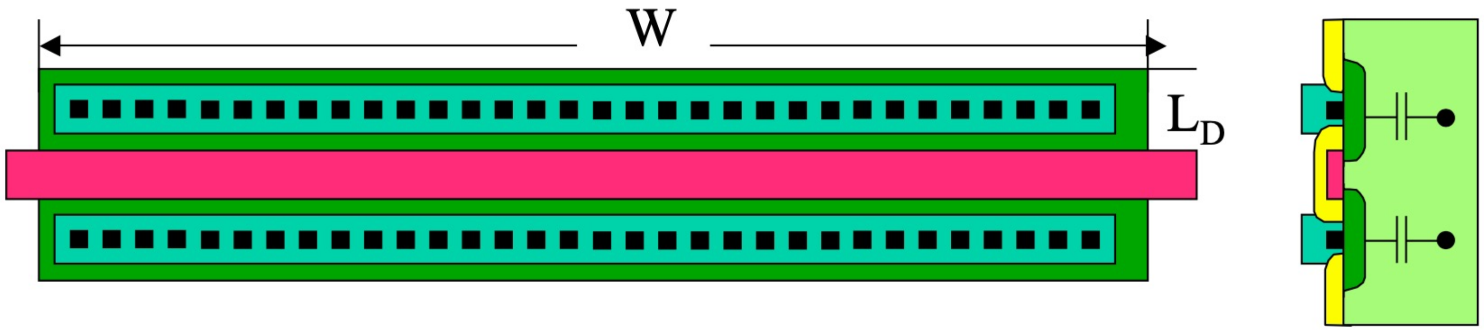
MOS Transistors: Fingers



Lienig, Scheible, “Fundamentals of Layout Design for Electronic Circuits,” Springer 2020.

Transistor Parasitics

- Analog transistors often have a large W/L ratio



- Capacitance diffusion substrate

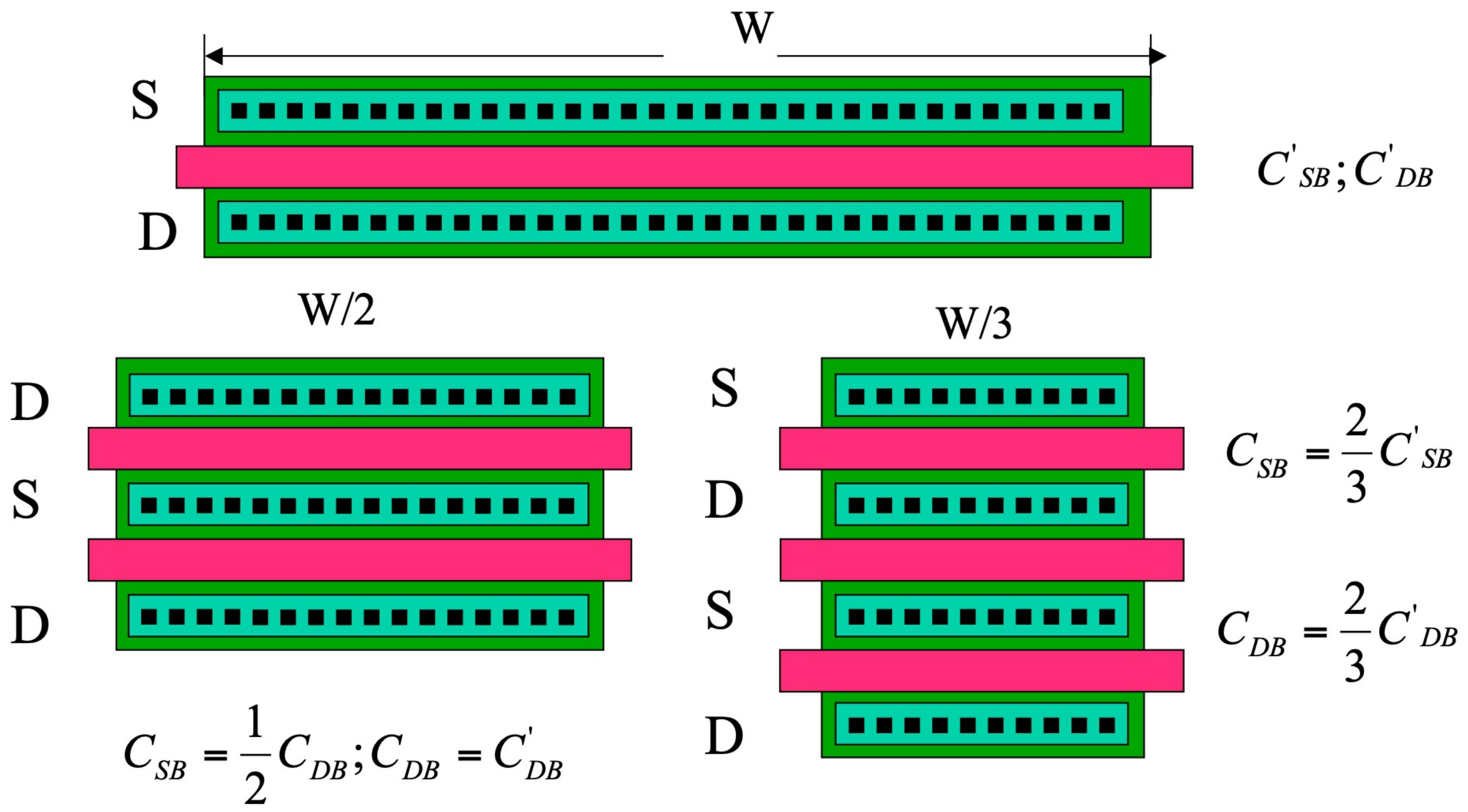
$$C_{SB} = C_{DB} = (W + 2l_{diff})(L_D + 2l_{diff})$$

- Resistance of the poly gate

$$R_{gate} = L_{gate} R_{sq,poly}$$

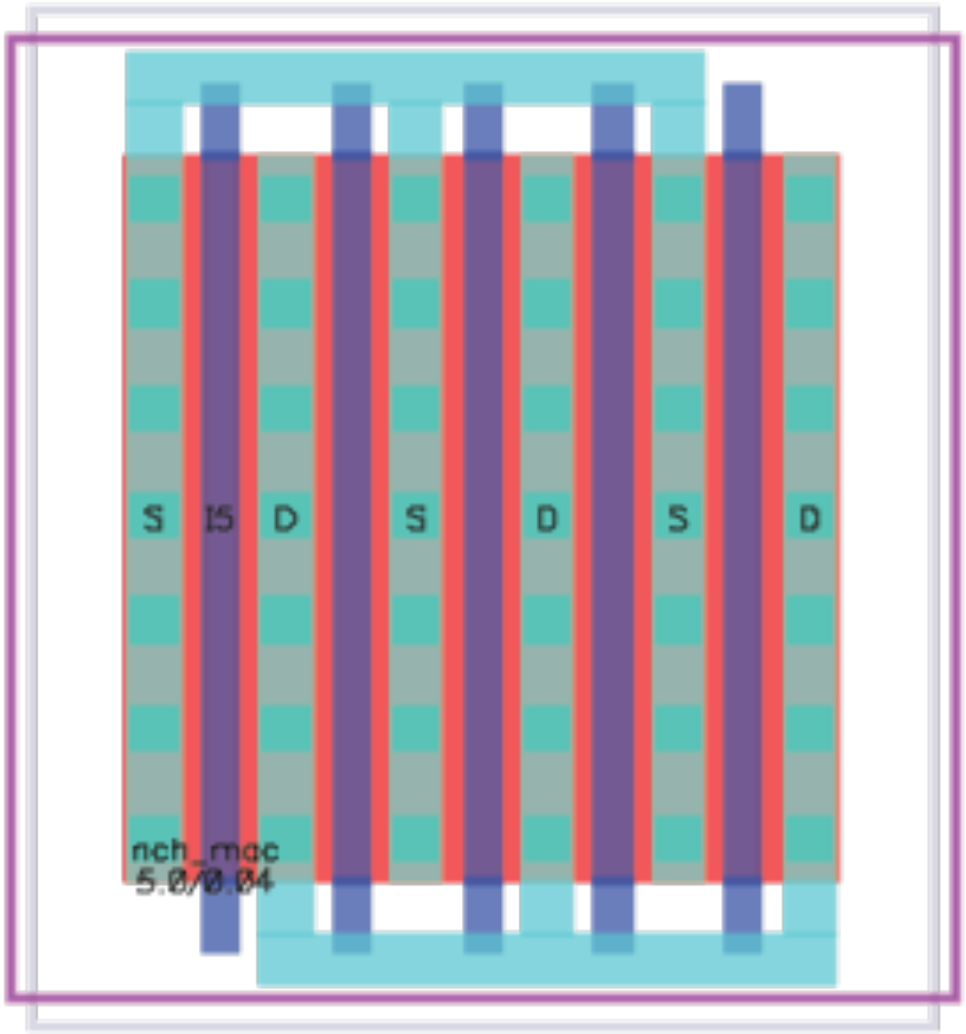
Maloberti, F, “Layout of Analog CMOS Integrated Circuits” (Part 2)

Capacitance Reduction (Shared Junctions)

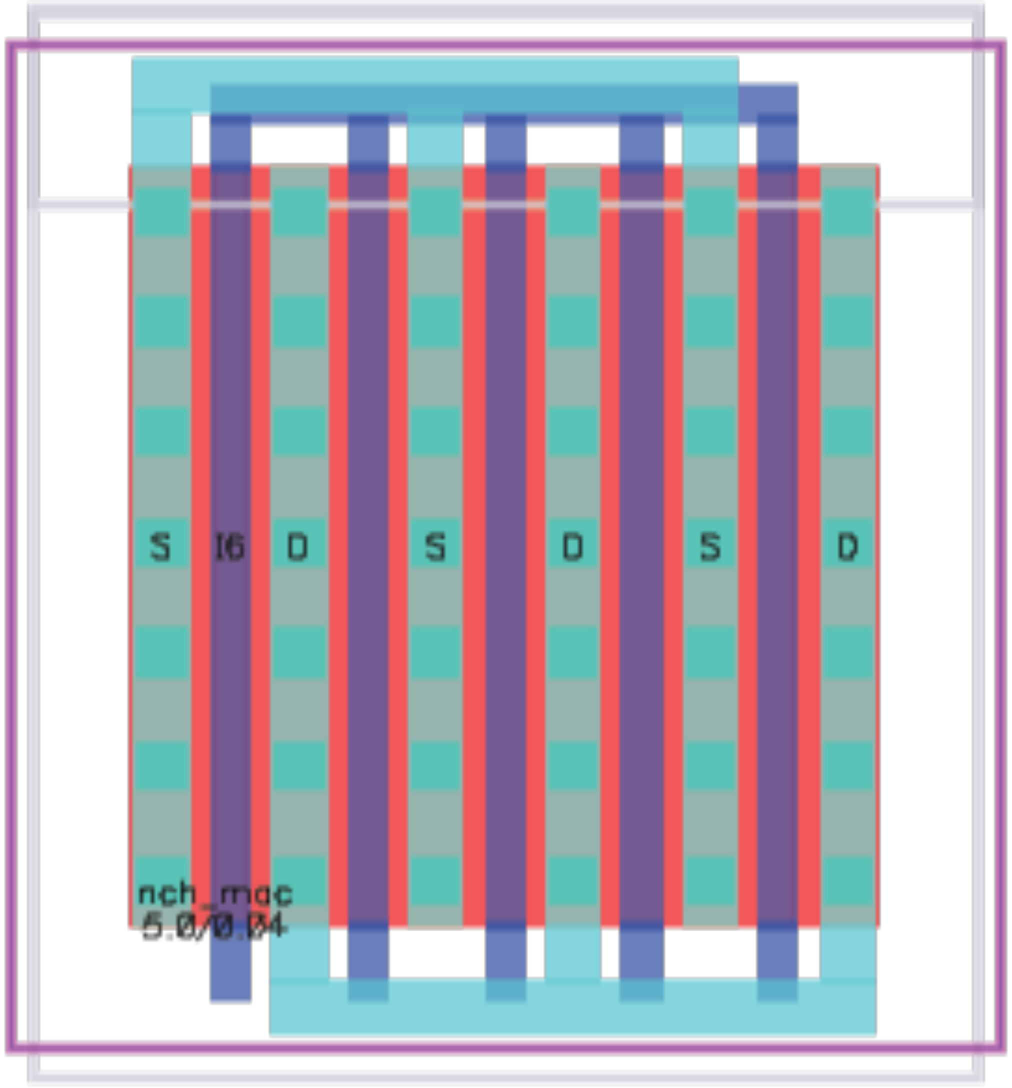


Maloberti, F, "Layout of Analog CMOS Integrated Circuits" (Part 2)

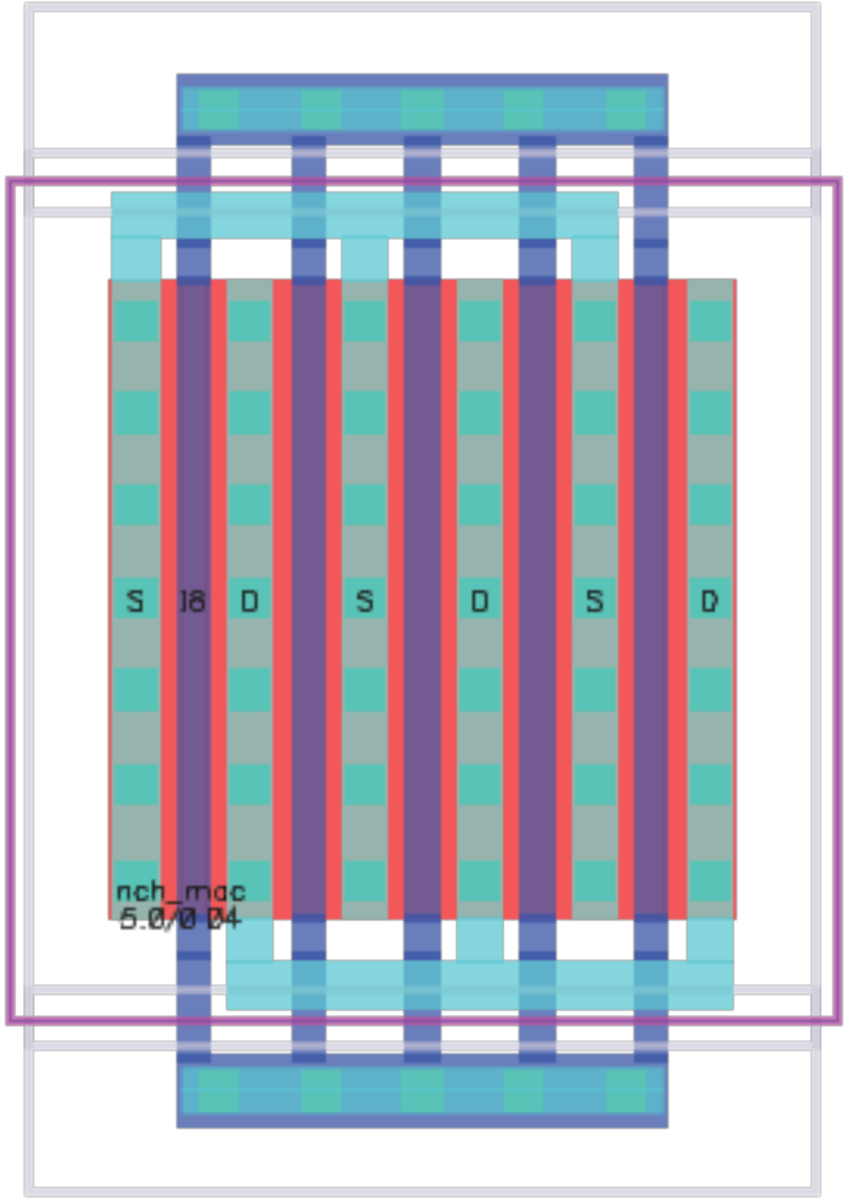
Connect Source Drain



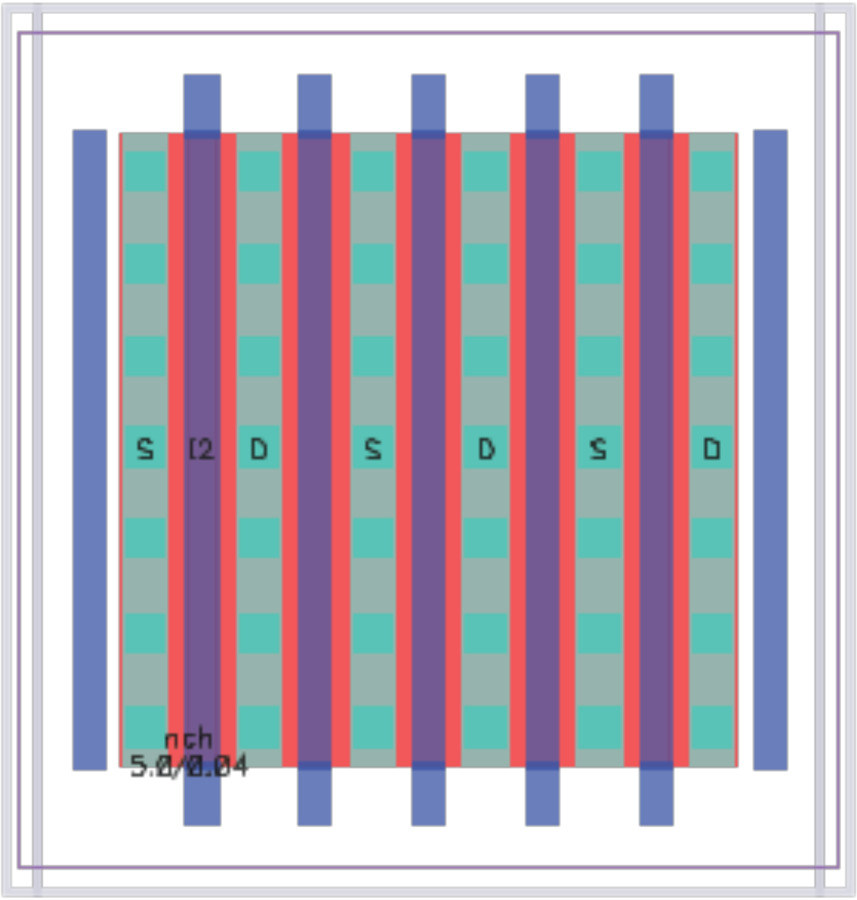
Connect Gate



Double-Sided Gate Contact



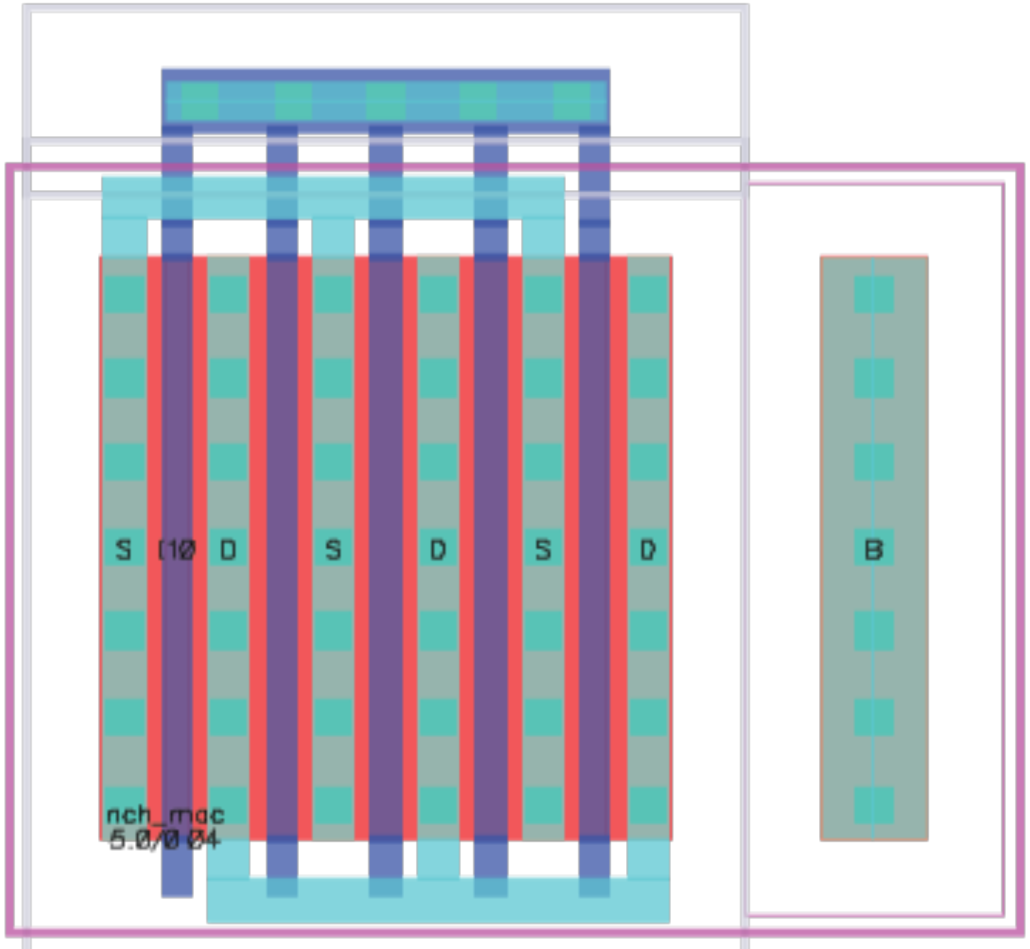
Dummy Fingers – Not so Dumb



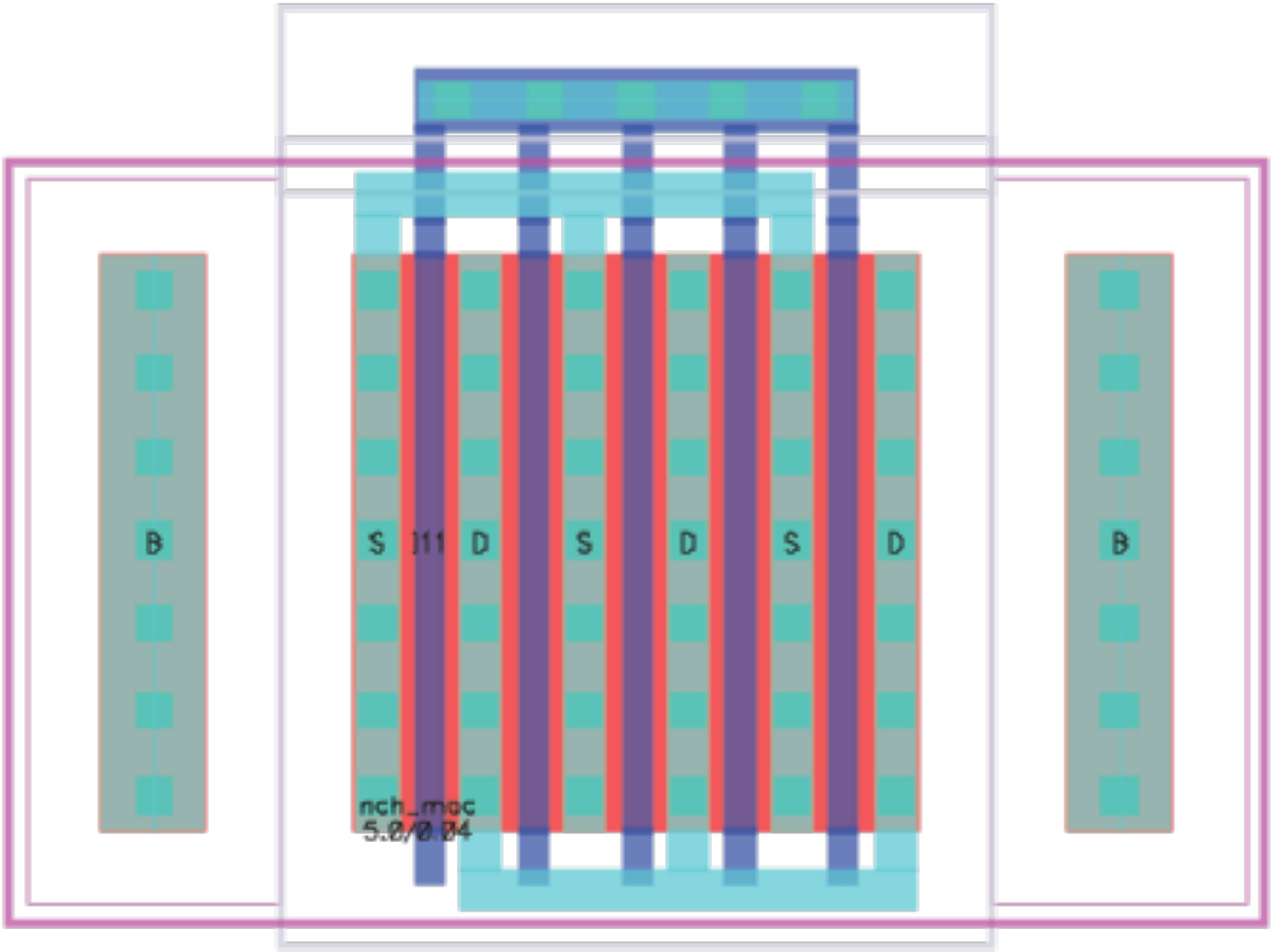
- TSMC DK does not ground dummy fingers and uses floating dummies
- If you use your own real transistor dummy fingers, ground (supply for PMOS) the gates and short (supply) the unused junctions.
- Make sure you place dummy in schematic
  - Needed for LVS (turn off ignore)
  - Good check that you don't have a layout error or short

Substrate and Body Contacts

Body Contact – It's 4 Terminals !



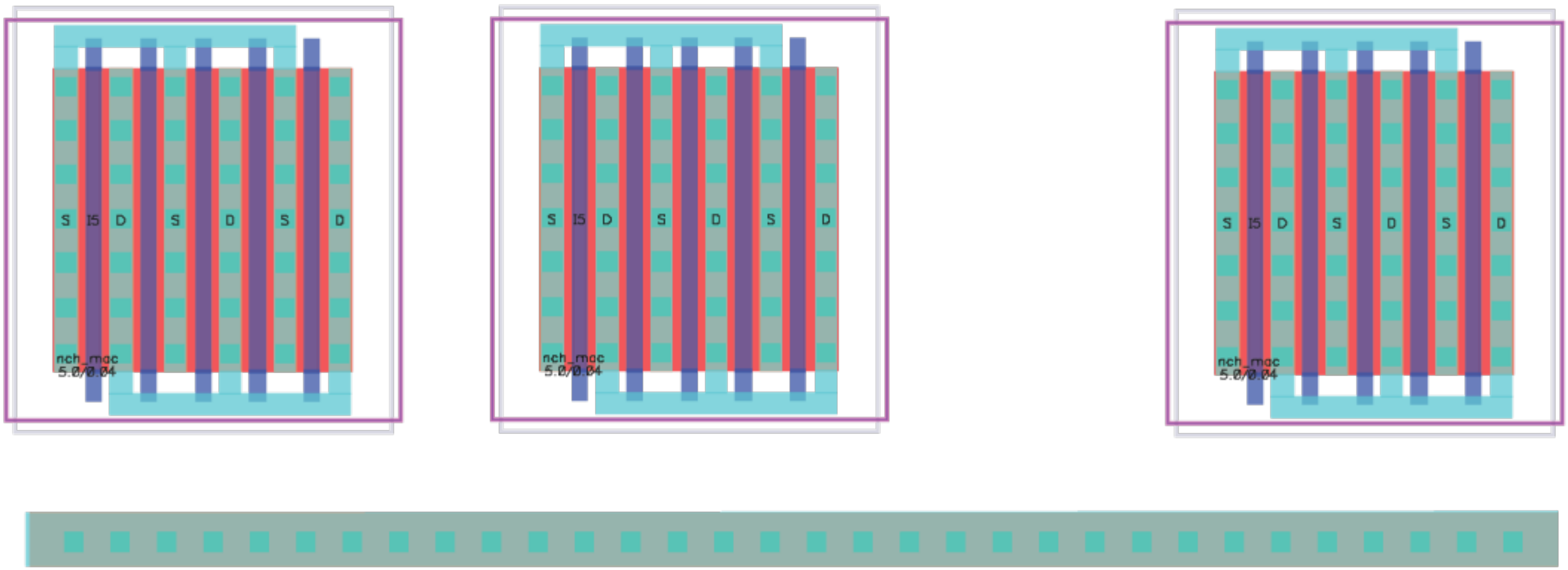
Double-Sided Detached Body



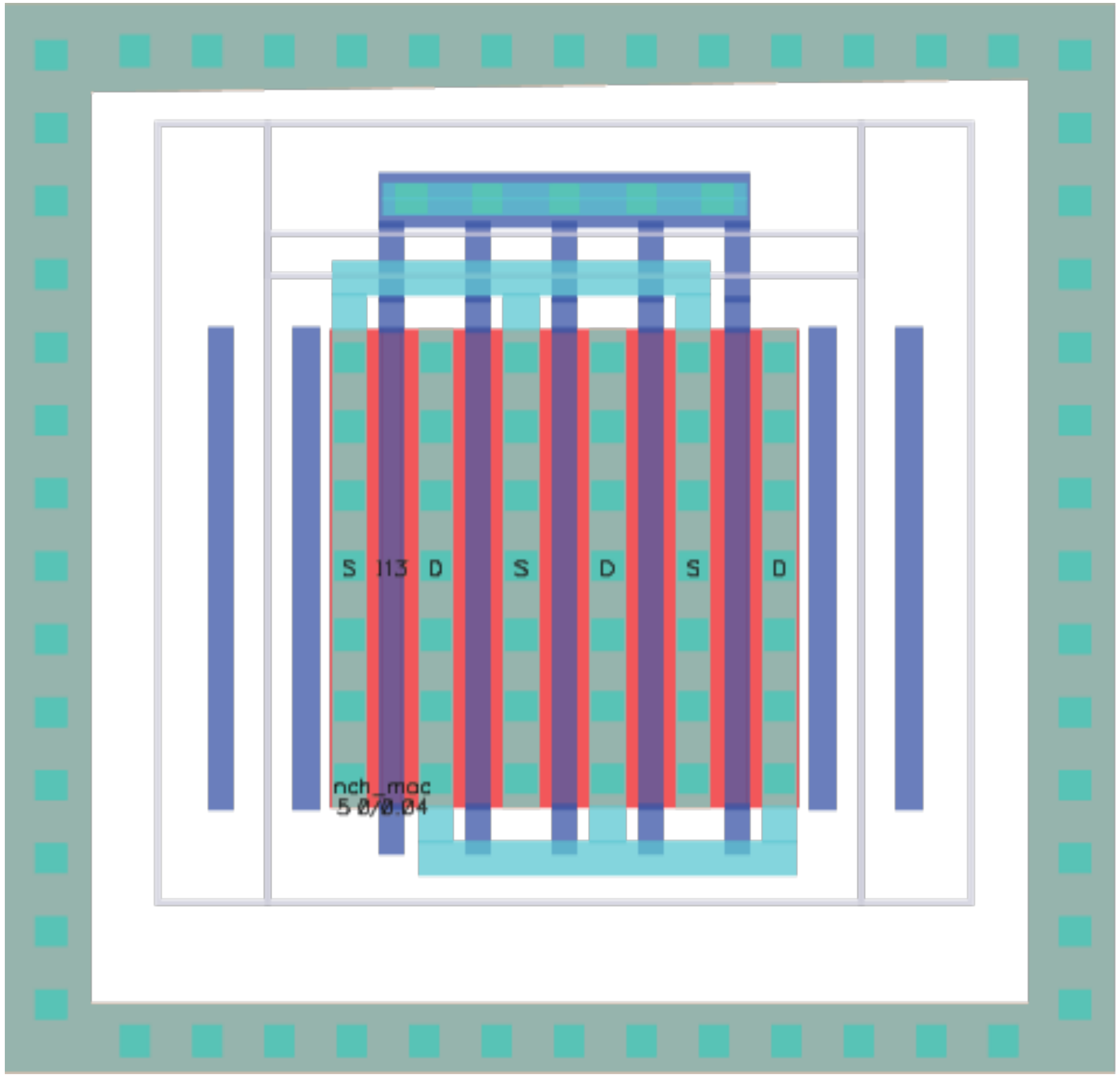
Can we attach body?

- To save area, we would like to put the body connection as close as possible
- When can we just “attach it” ?

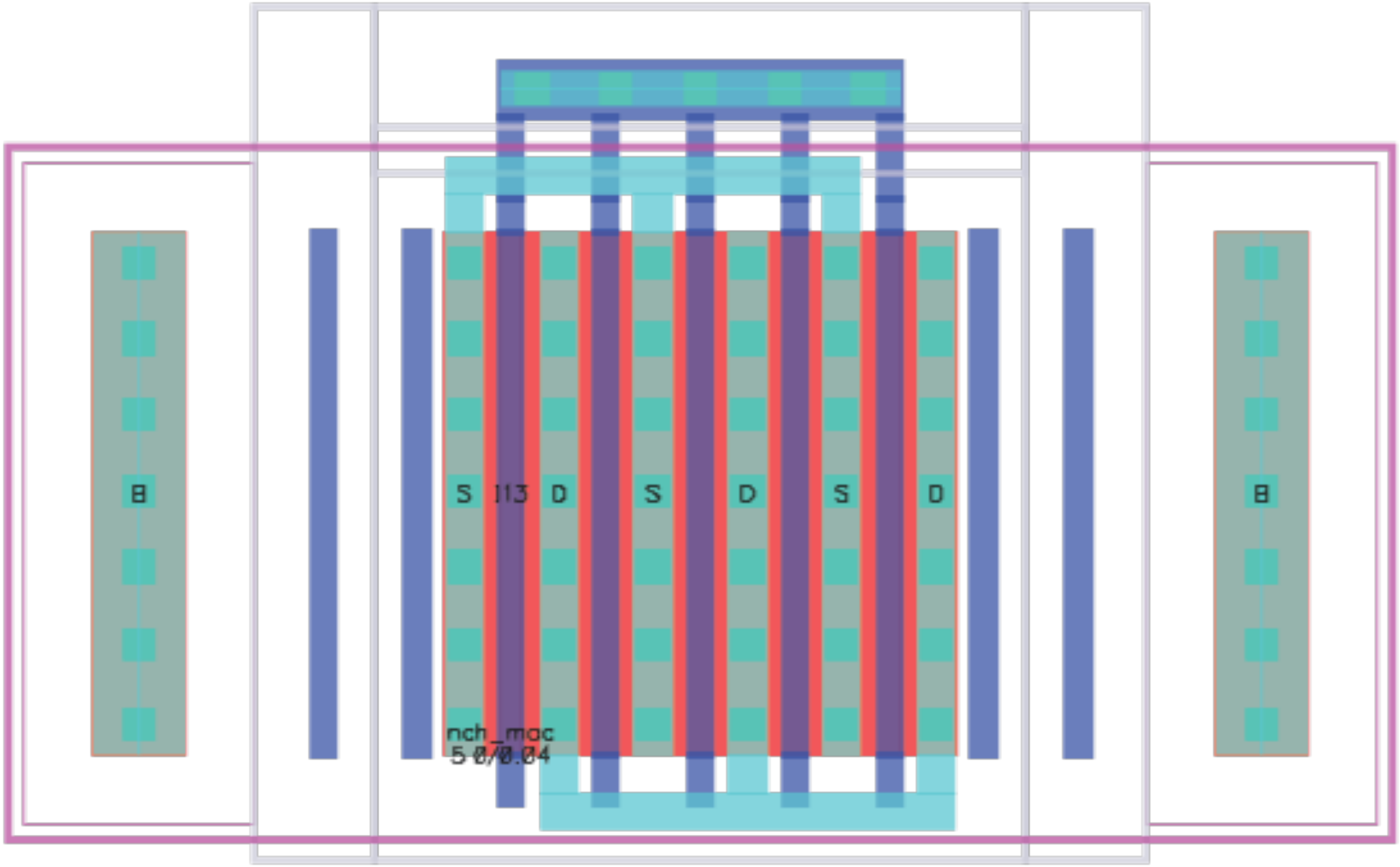
Horizontal Body



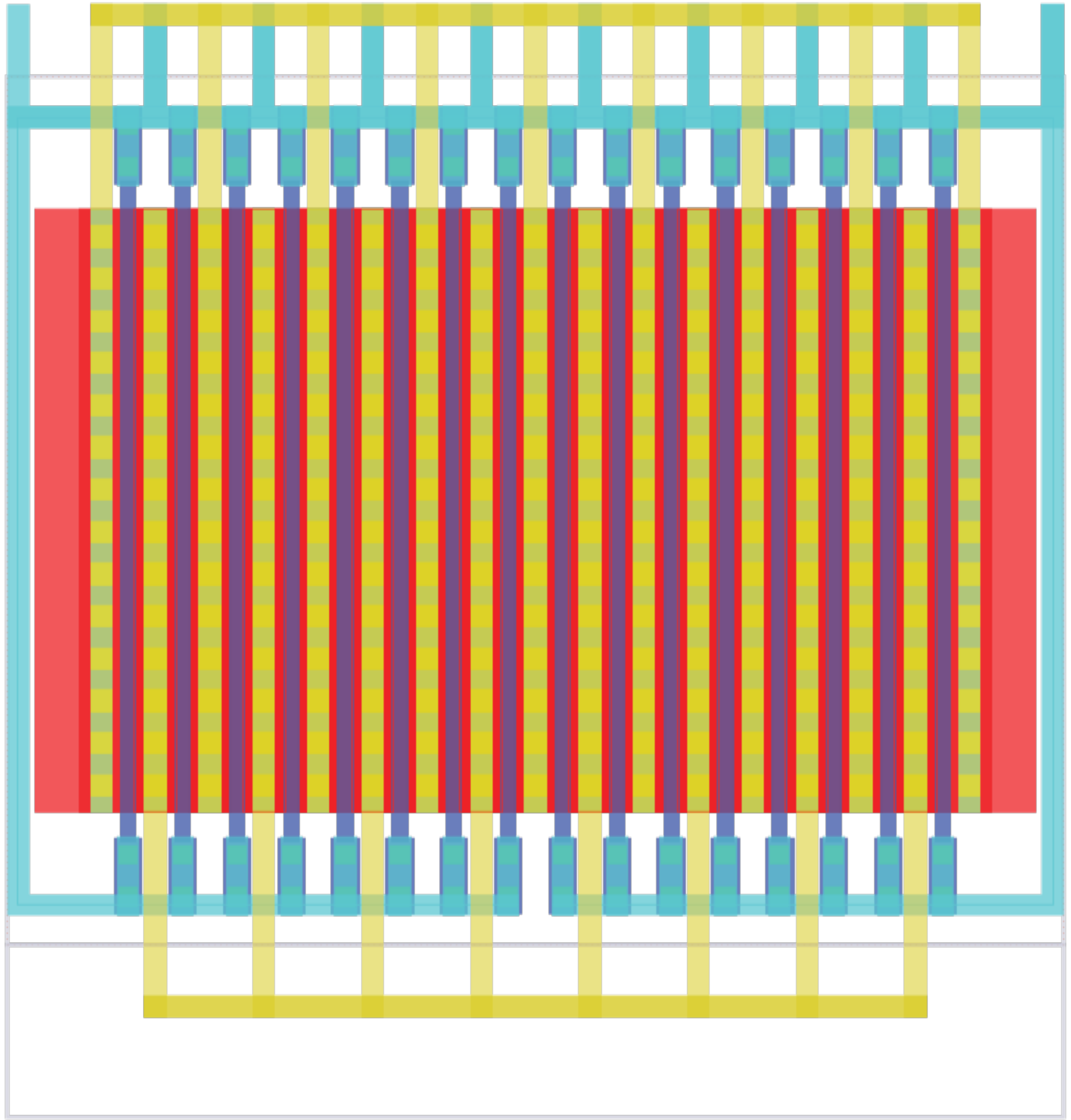
Ring



Full Layout

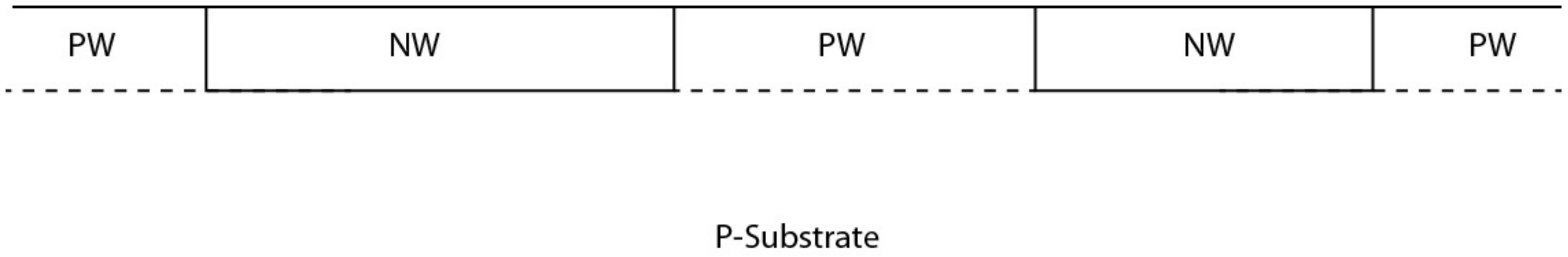


“RF” Layout (Substrate Tap Not Shown)



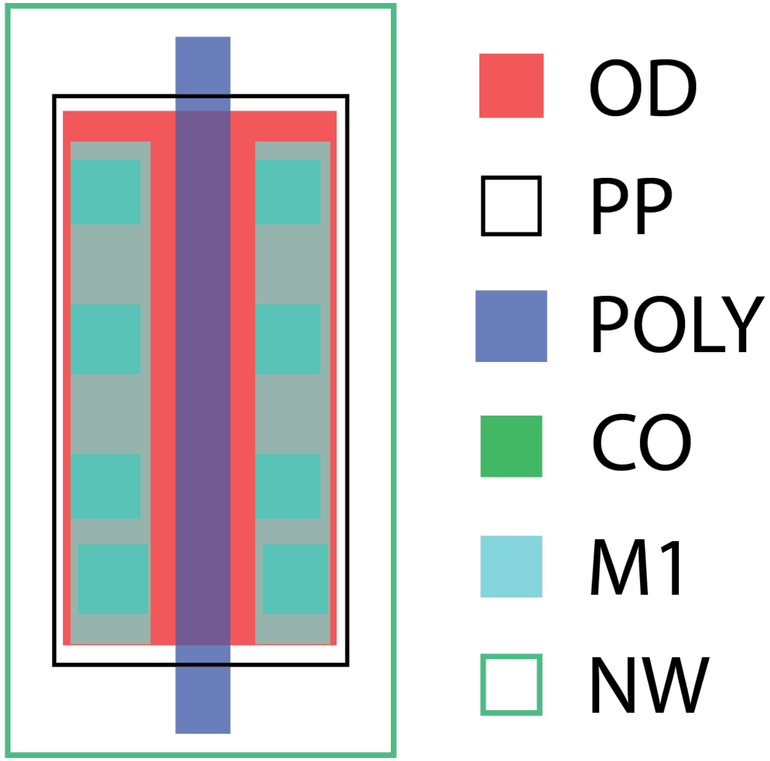
WELLS

Normal N-Well (NW) Structure



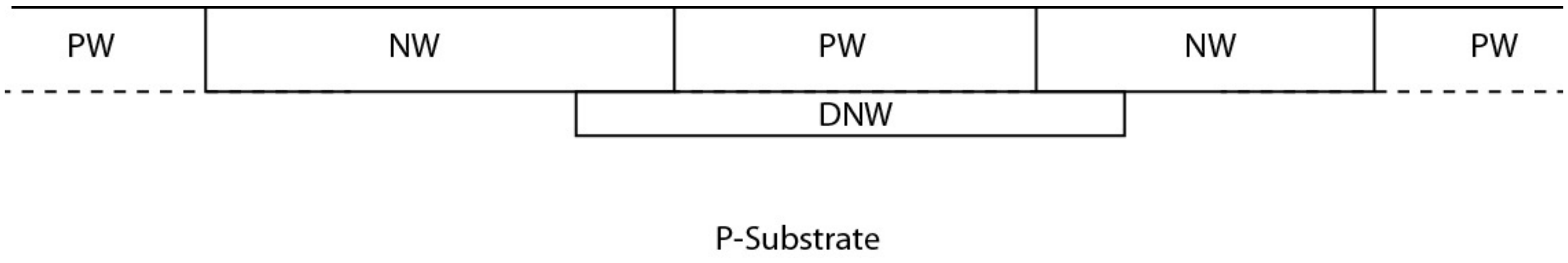
- During normal layout, everywhere you specify an NW, n+ doping is used to create a well. Automatically, every other surface is converted to p+ or PW. This layer is not isolated and therefore NMOS devices are normally subject to substrate noise pickup.
- You can create an undoped layer with a well blocking layer (block P+ implant), useful for inductors to minimize eddy currents (magnetically induced currents), which de-Q the structures.

PMOS



- Place transistor in NW (don't forget to connect NW to ???)
- Dope it with PP (instead of NP)

Deep NWell (DNW) Structure

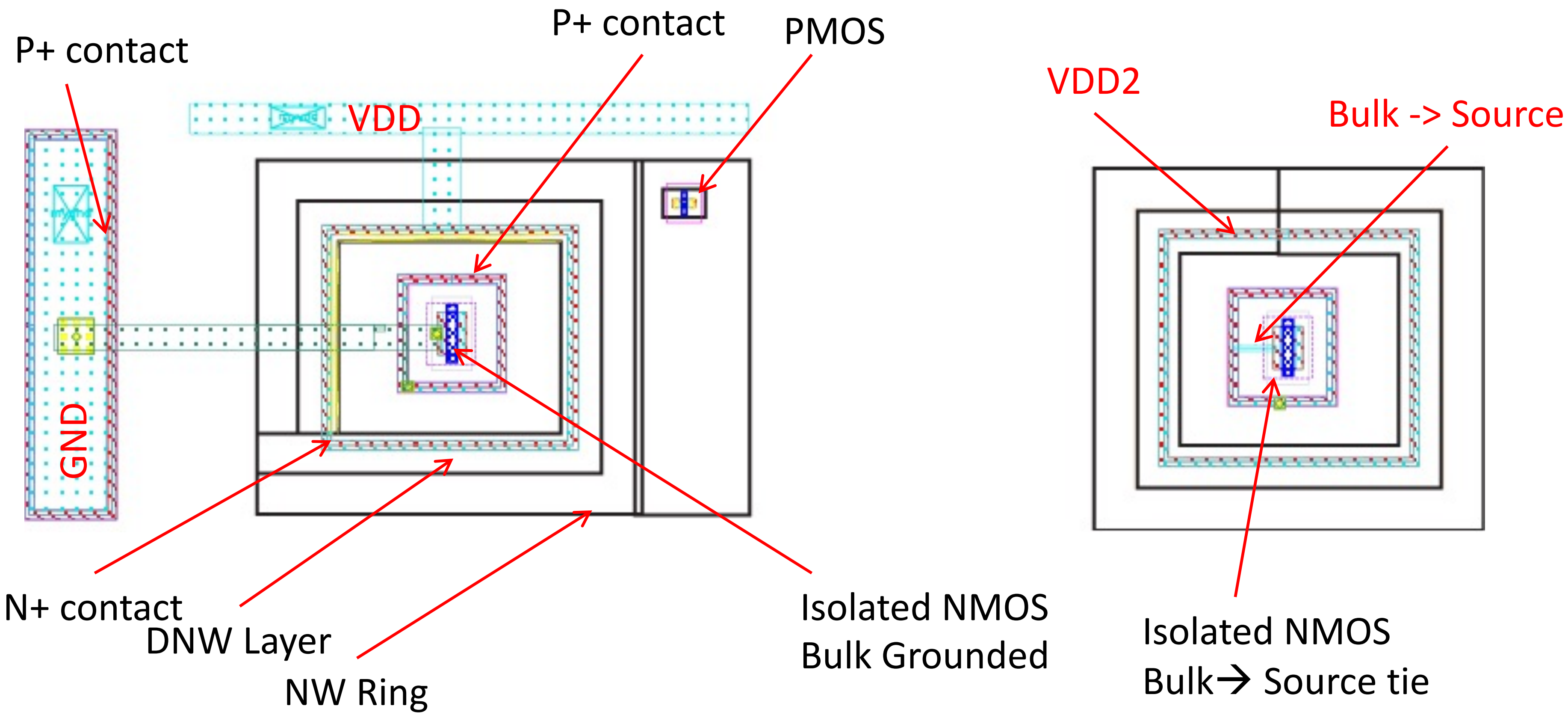


- The DNW device is an isolated NMOS in a regular twin well process.
- To create an isolated PW, a deep NW (DNW) is implanted underneath the PW.
- To isolate this structure, you must surround it by an overlapping NW (0.4um) so that it is electrically biased in order to isolate the PW. Connect this NW to the highest supply voltage to maximize the reverse bias and to minimize the well to substrate capacitance (to minimize noise pickup).

Isolated NMOS

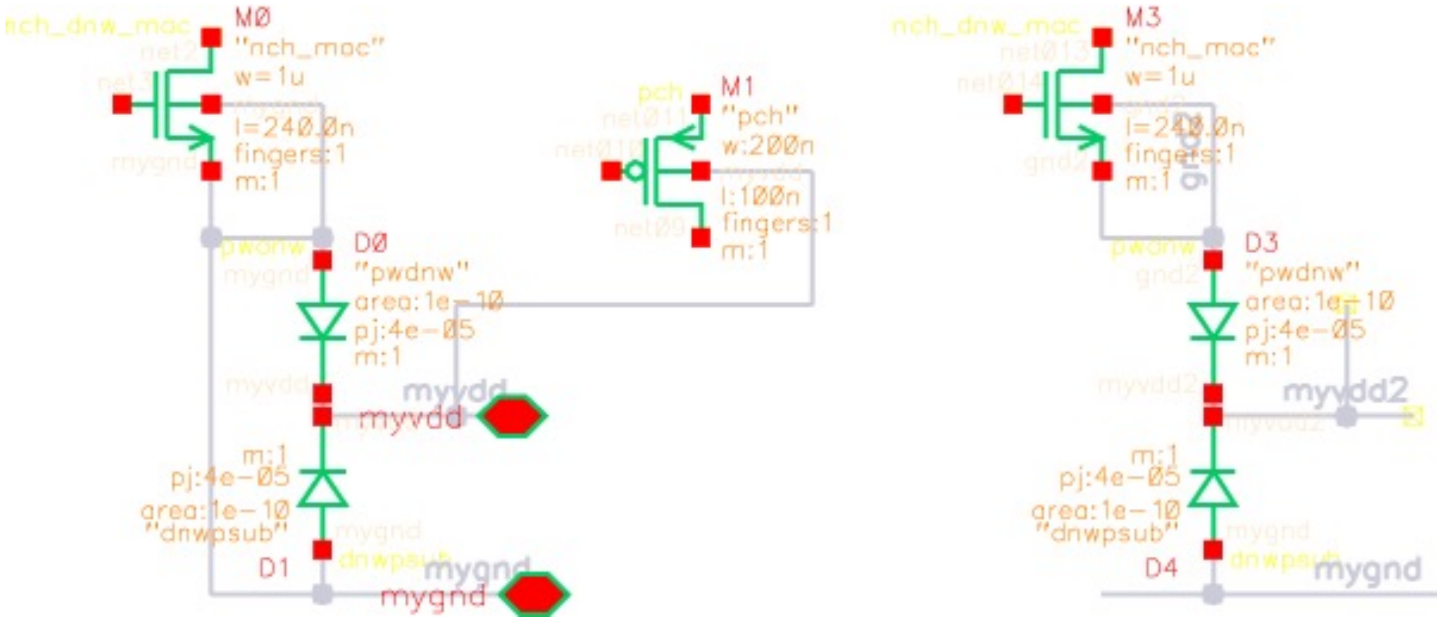
- You can layout isolated NMOS devices using the _dnw transistors or by converting regular NMOS transistors. Use the guidelines given in the next page.
- Note that the isolated NMOS can have its bulk tied to ground or to its source. If you tie it to the source, make sure you extract the well capacitances (which can be large!) and simulate AC performance.
- If you need to make a bulk-to-source connection, you should layout an optimized small well rather than sharing the device with other transistors in a big well.

Layout of DNW Transistors



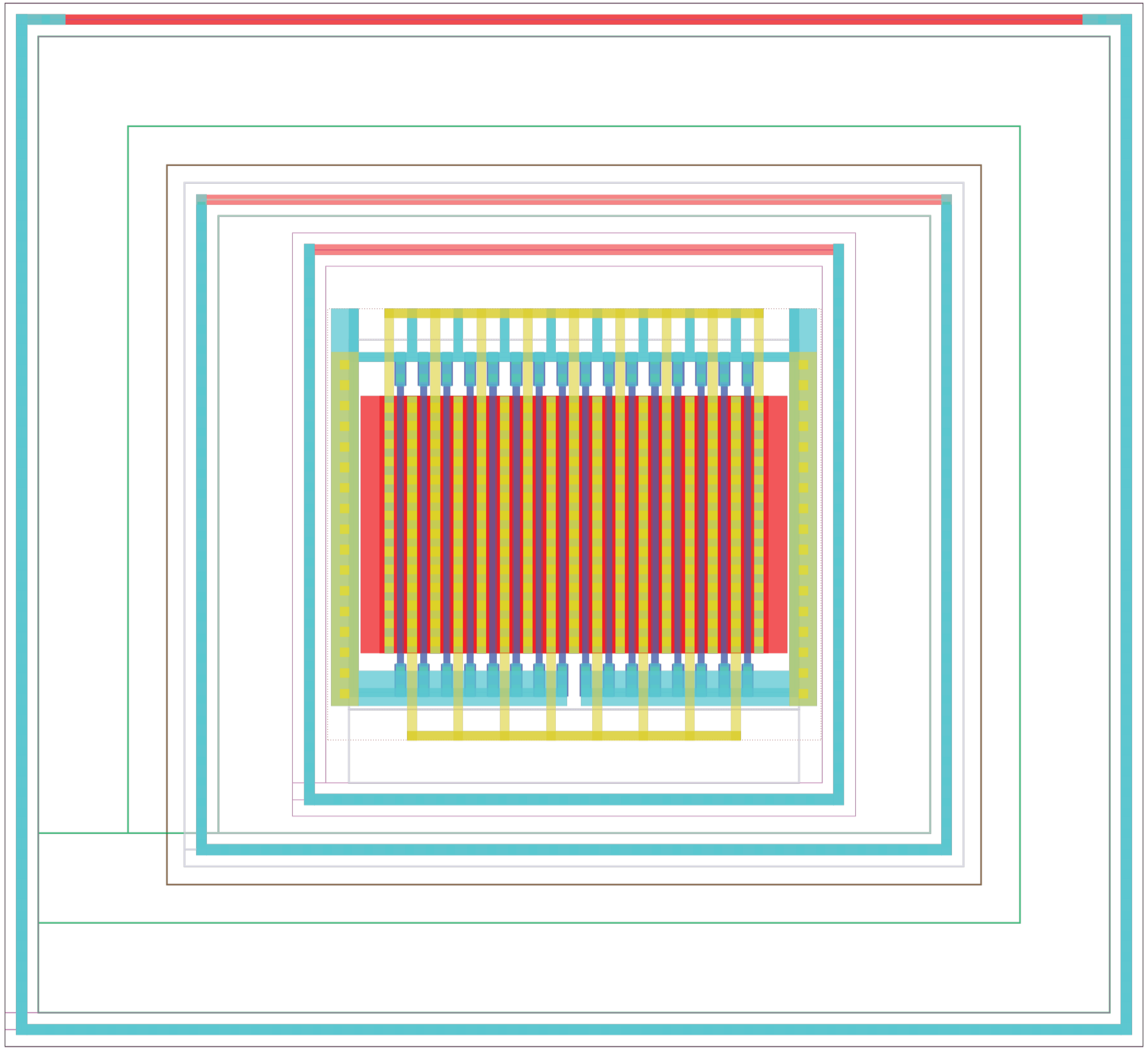
- You MUST have a closed NW ring around the device for the extraction to correctly pick up a different voltage domain (VDD2 above)
- You must have a substrate tie near the device (GND)

Schematics



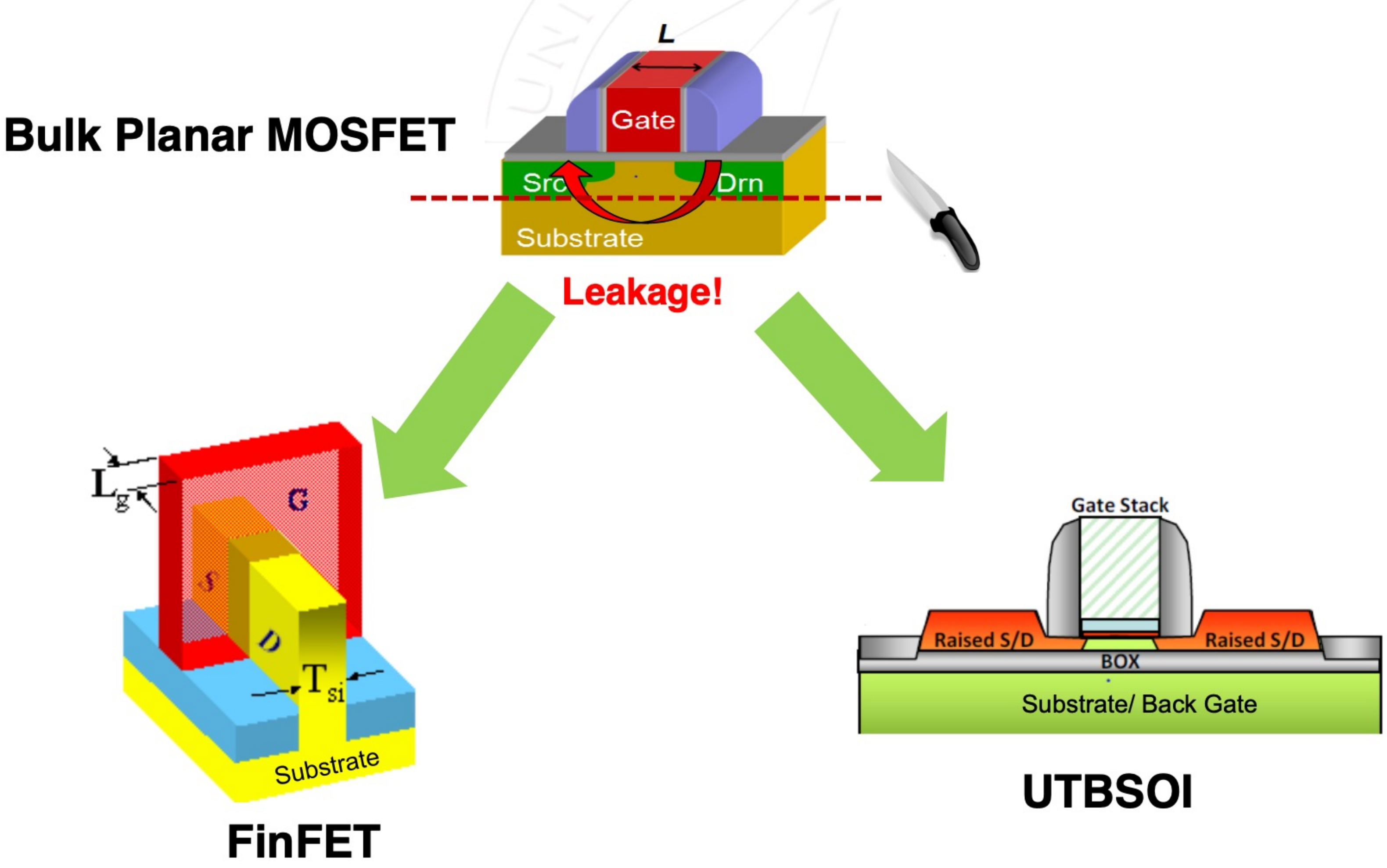
- This schematic matches the previous layout.
- Two diodes are extracted, one for the NW (dnwpsub), and a second diode from the PWELL to the DNW (pwdnw)
- Note the first device has the bulk of the NMOS grounded whereas the second device has bulk tied to source.
- The second device is completely isolated from the substrate (mygnd) at DC

5T or 6T Device



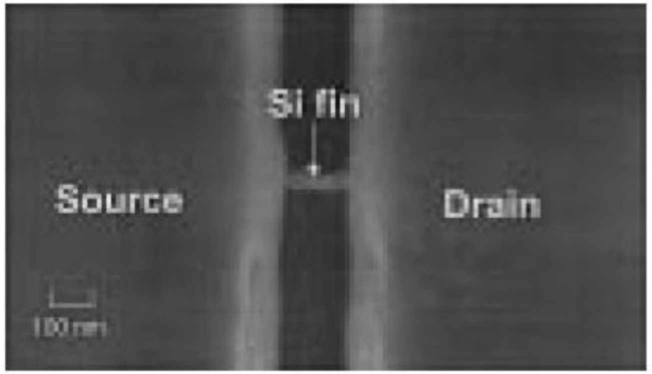
FinFETs

New MOSFET Structures

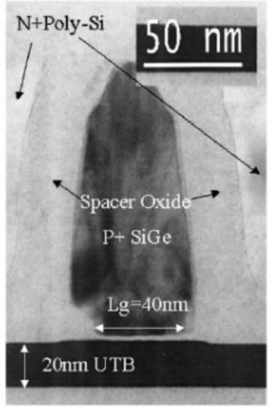


Early Demonstrations

[redacted] [redacted]

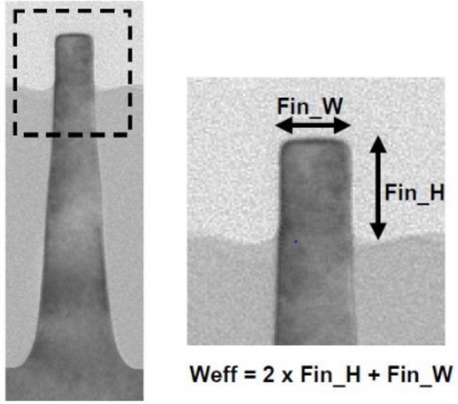


X. Huang et al. IEDM 1999 (**UC Berkeley**)



Y. Choi et al. IEEE EDL 2000- (**UC Berkeley**)

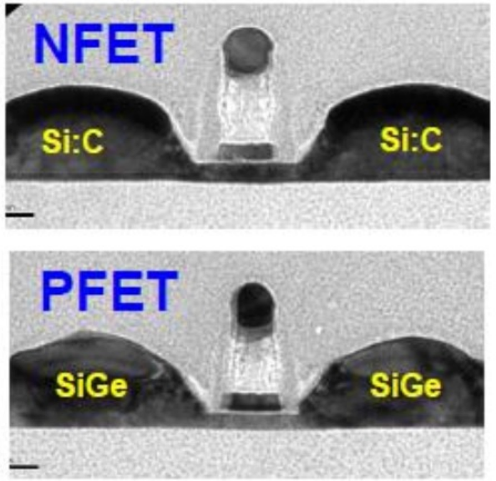
FinFET



Weff = 2 x Fin_H + Fin_W

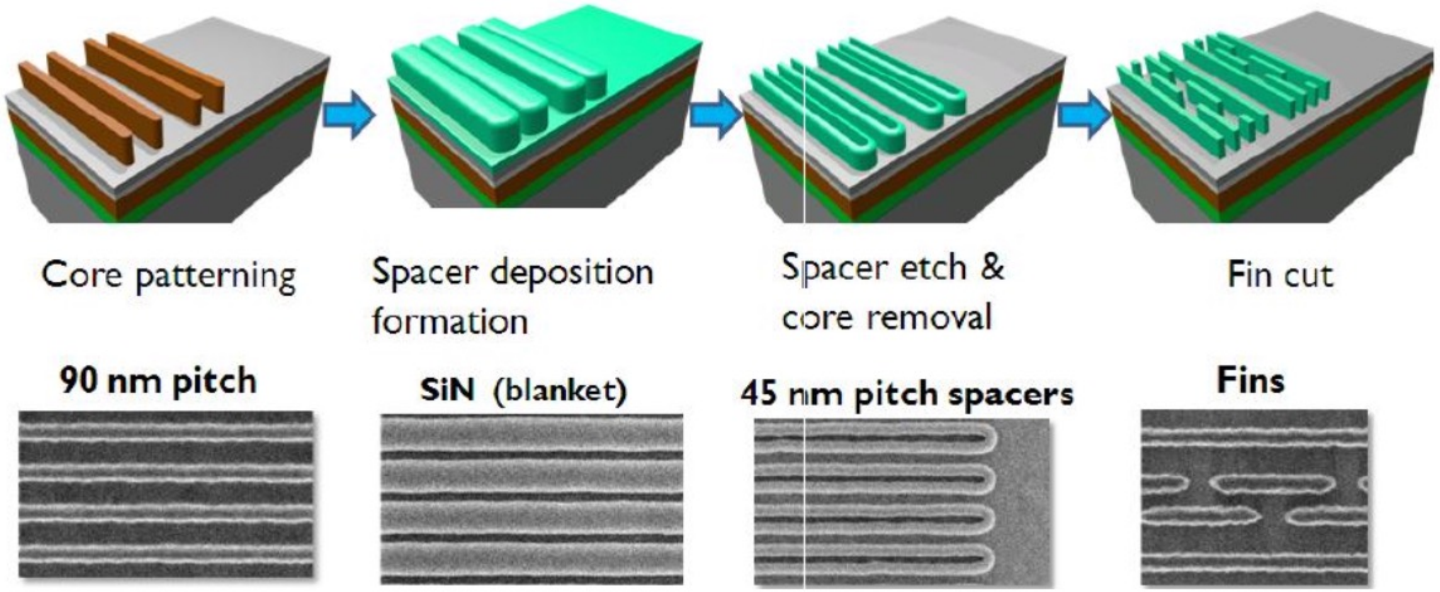
C.C. Wu et al. IEDM 2010 (TSMC)

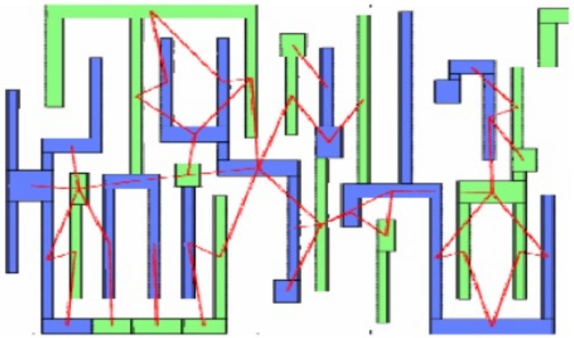
UTBSOI



K. Cheng et al. IEDM 2009 - (IBM / ST)

Creating the fins – Double Patterning



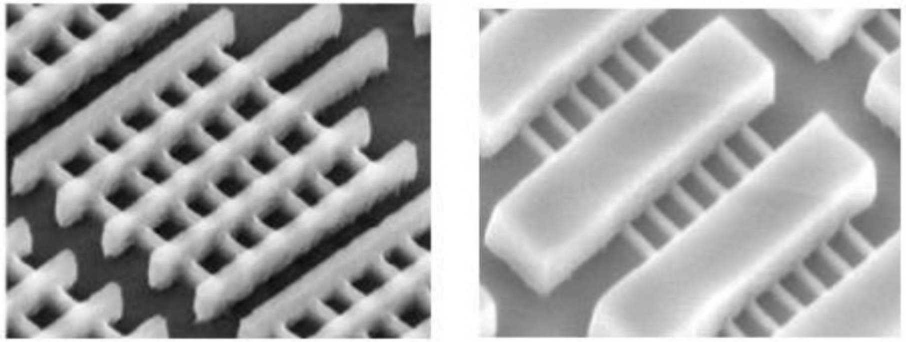


Dual color layout

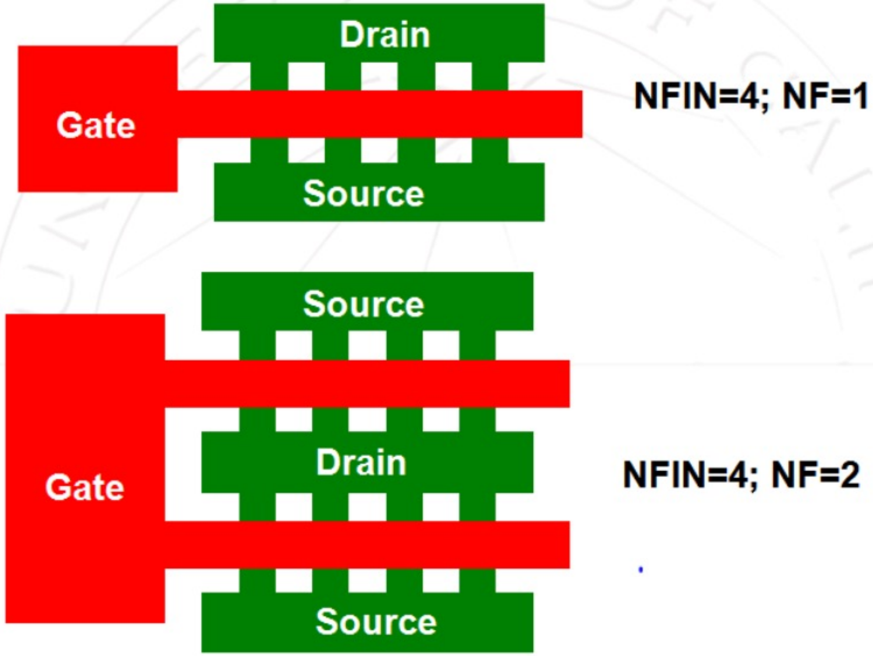
- Sidewall Image Transfer based lithography used to create closely spaced thin Fins
- Next technology node => finer lithography
  - Options: triple patterning, EUV, multi-beam electron lithography
- In 20/14nm Double patterning extended to Poly and M1 also
  - Dual color assignment in layout for these layers (M1A & M1B)

NF vs NFIN in FinFETS

- Width is quantized in FinFETs
  - Can only be integer multiples of ($2H_{FIN}+T_{FIN}$)
  - H_{FIN} and T_{FIN} are currently technology constants
- Device can have many Fins (NFIN)
  - And multiple fingers as in bulk planar FETs (NF)

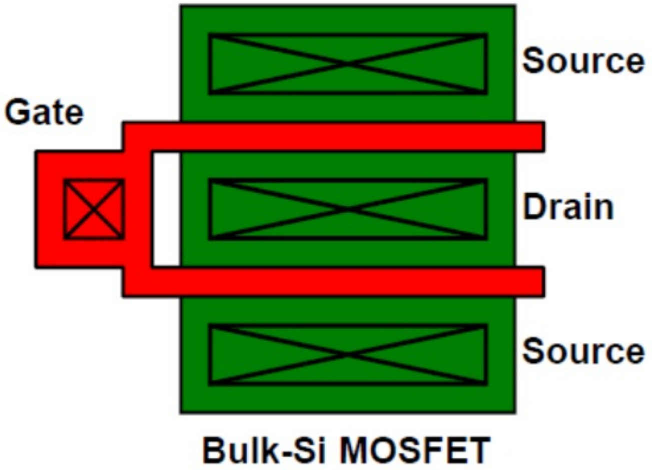


22nm, Intel, IEDM2012

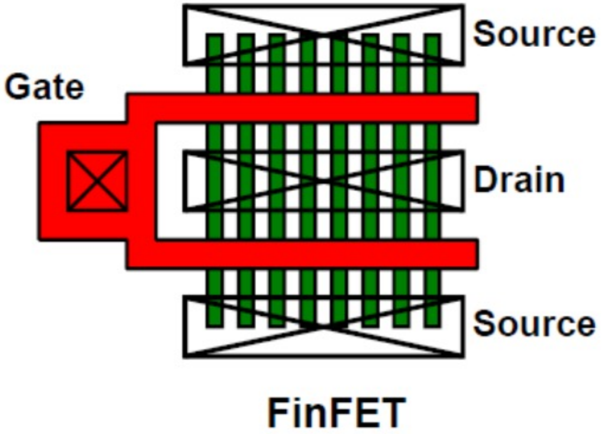


NF vs NFIN in FinFETs (cont)

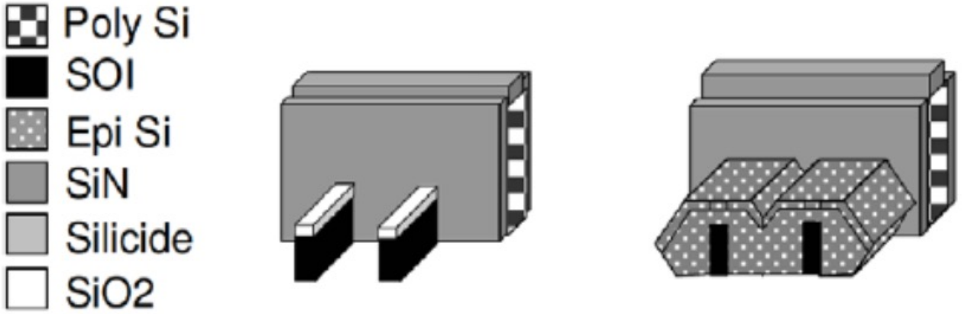
- Layout is similar to Bulk-planar FET except that width is quantized



$W_{eff} = (2 * H_{fin}) * N_{Fins} * N_{Gate\text{-}fingers}$

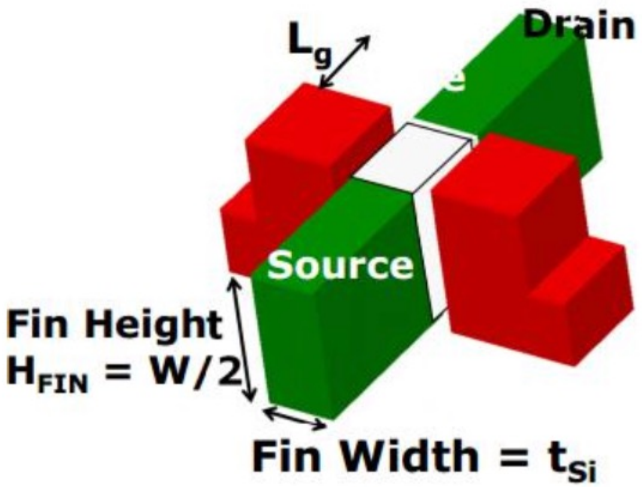


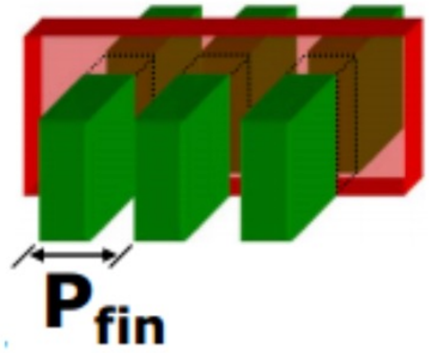
- Source/Drain contact is for multiple fins is merged into one using selective epitaxial regrowth



FinFET Device Design Tradeoffs

- Fin Width (T_{FIN})
  - Thinner Fin has better short channel effects control
- Fin Height (H_{FIN})
  - Limited by Etching Tech
- Fin Pitch
  - Limited by lithography
  - Parasitic Resistance and Cap heavily depend of Fin Pitch





T.J. King, ISSCC2013 Forum

Layout Editing Concepts

- Polygons
  - Merge
  - Chop
- F4 → options
- Array Copy vs Tile
- Vias
- Stretching / Edges
- Live DRC / DRD editing
- MPP's (Multi-Part Path)
- Grouping vs Hierarchy
  - Edit in place
- Bus layout

- Learn to Probe Nets / Mark Nets
- Learn how to do a hierarchy copy (and modify cells to point to new cells)

References

- Lienig, Scheible, “Fundamentals of Layout Design for Electronic Circuits,” Springer 2020.
- Maloberti, F, “Layout of Analog CMOS Integrated Circuits” (Part 2)
- Hastings, “The art of analog layout,” Prentice Hall, 2001.