https://ucberkeleyee290c.github.io/sp22/

EE290C: 28nm SoC for IoT

The Layout Lecture: Virtuoso Lecture

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- Please do not post these slides on the Internet. There are no "secrets" in these slides, but they contain some actual layouts from protected technologies.

Topics

Part 0: The virtuoso basics (this lecture)

Part 1

- Layout of a FET 3T
  - Dimensions, fingers, dummy
  - DFM
- PMOS vs NMOS
- Body contacts 4T
- DNW and 5T and 6T transistors

Part 2

- Analog Layout
  - Matching
  - Common centroid
  - Symmetry
  - Unit Cell Concept
- Current Source
- Differential Pair

Part 3

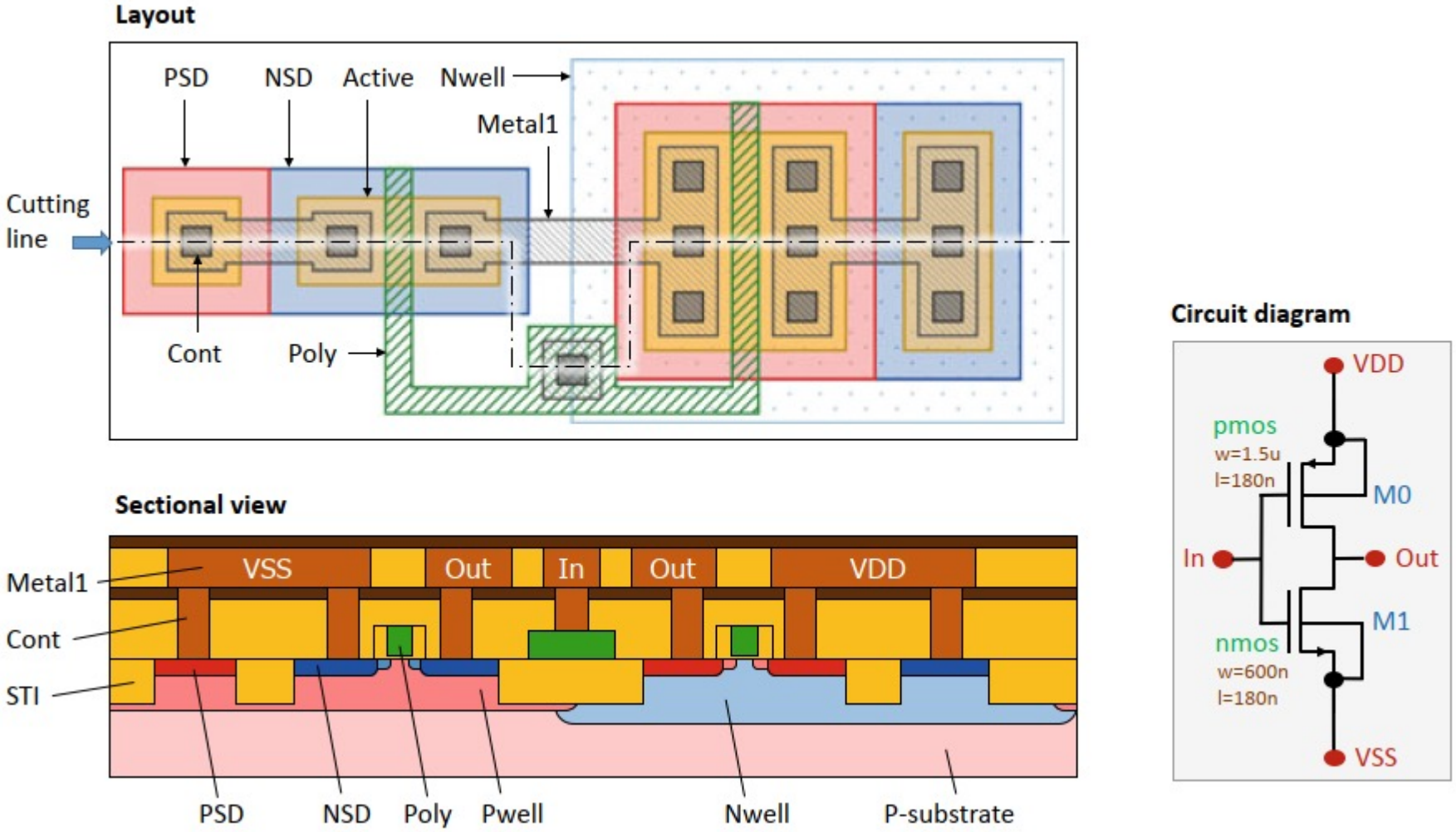
- Capacitors
  - Love your MOM
- Resistors
- More arrays
- Inductors
- Electromigration Rules
- Antenna Rules
- Examples:
  - DAC
  - Op-Amp
  - Tiles of blocks
  - Pin placement
- Layout Hierarchy vs Schematic

https://ucberkeleyee290c.github.io/sp21/

Layout Tutorial: Overview

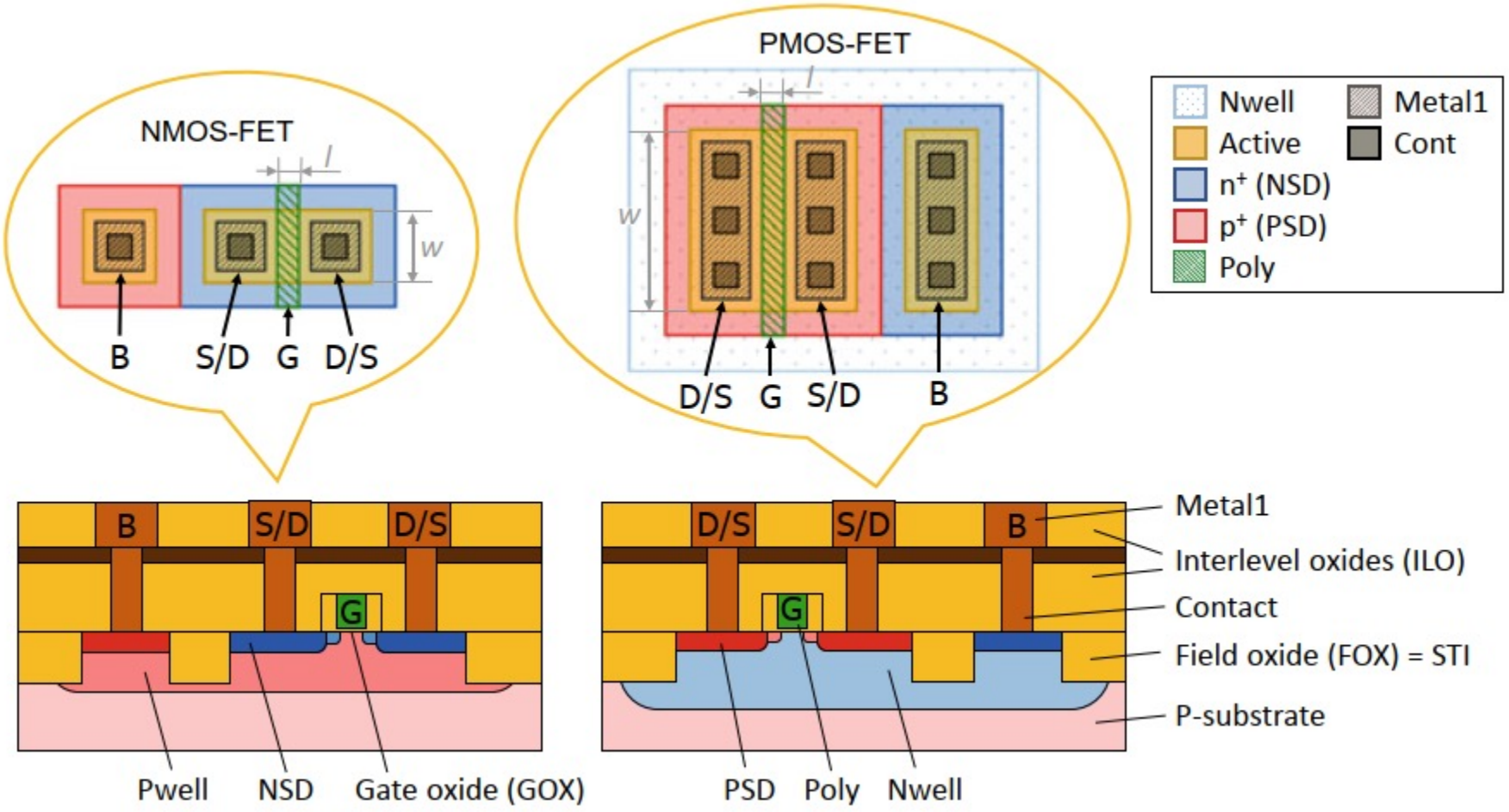
Layout

- Lienig, Scheible, "Fundamentals of Layout Design for Electronic Circuits," Springer 2020.



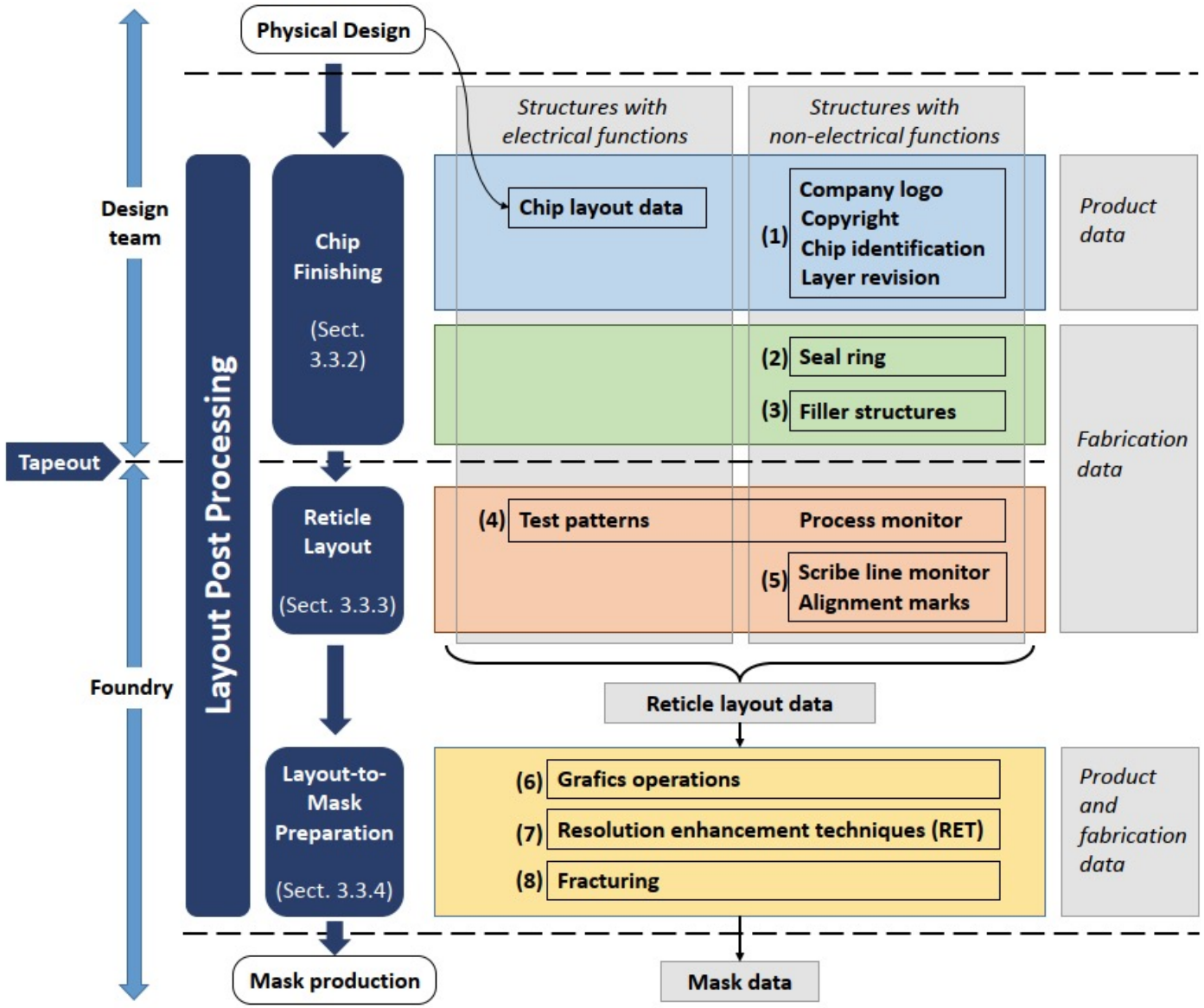
Lienig, Scheible, "Fundamentals of Layout Design for Electronic Circuits," Springer 2020.

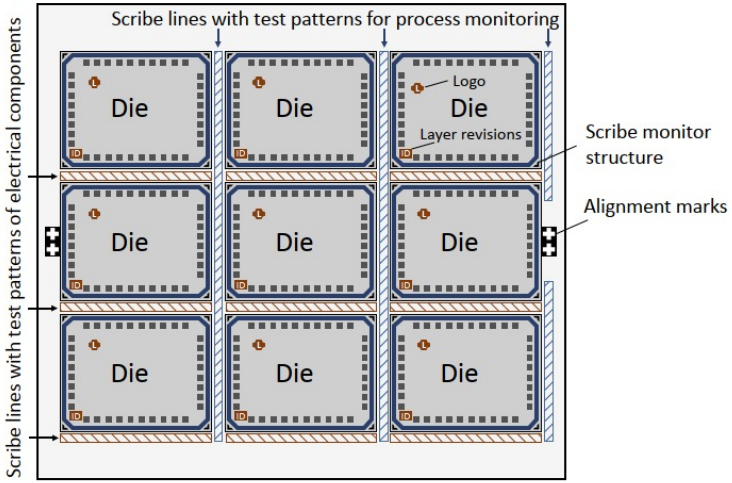
Layers



Lienig, Scheible, "Fundamentals of Layout Design for Electronic Circuits," Springer 2020.

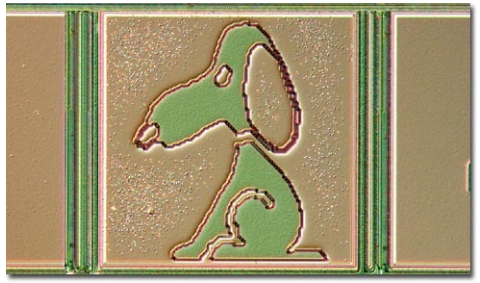
Processing

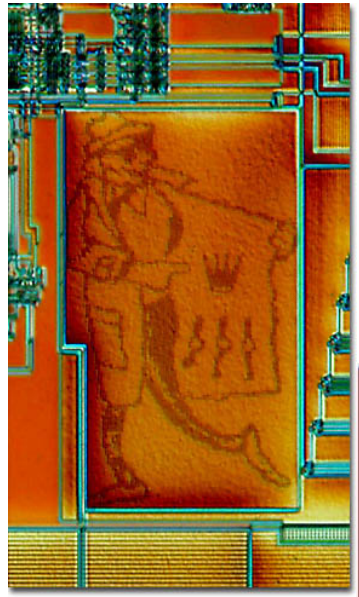

Physical Design
Design team
Chip Finishing
(Sect. 3.3.2)
Tapeout
Reticle Layout
(Sect. 3.3.3)
Foundry
Layout Post Processing
Layout-to-Mask Preparation
(Sect. 3.3.4)
Mask production
Structures with electrical functions
Structures with non-electrical functions
Chip layout data
(1) Company logo
Copyright
Chip identification
Layer revision
Product data
(2) Seal ring
(3) Filler structures
Fabrication data
(4) Test patterns
Process monitor
(5) Scribe line monitor
Alignment marks
Reticle layout data
(6) Grafics operations
(7) Resolution enhancement techniques (RET)
(8) Fracturing
Product and fabrication data
Mask data


Scribe lines with test patterns for process monitoring
Scribe lines with test patterns of electrical components
Die
Logo
Layer revisions
Scribe monitor structure
Alignment marks

Company Logos and Stuff

- https://micro.magnet.fsu.edu/creatures/logoindex.html

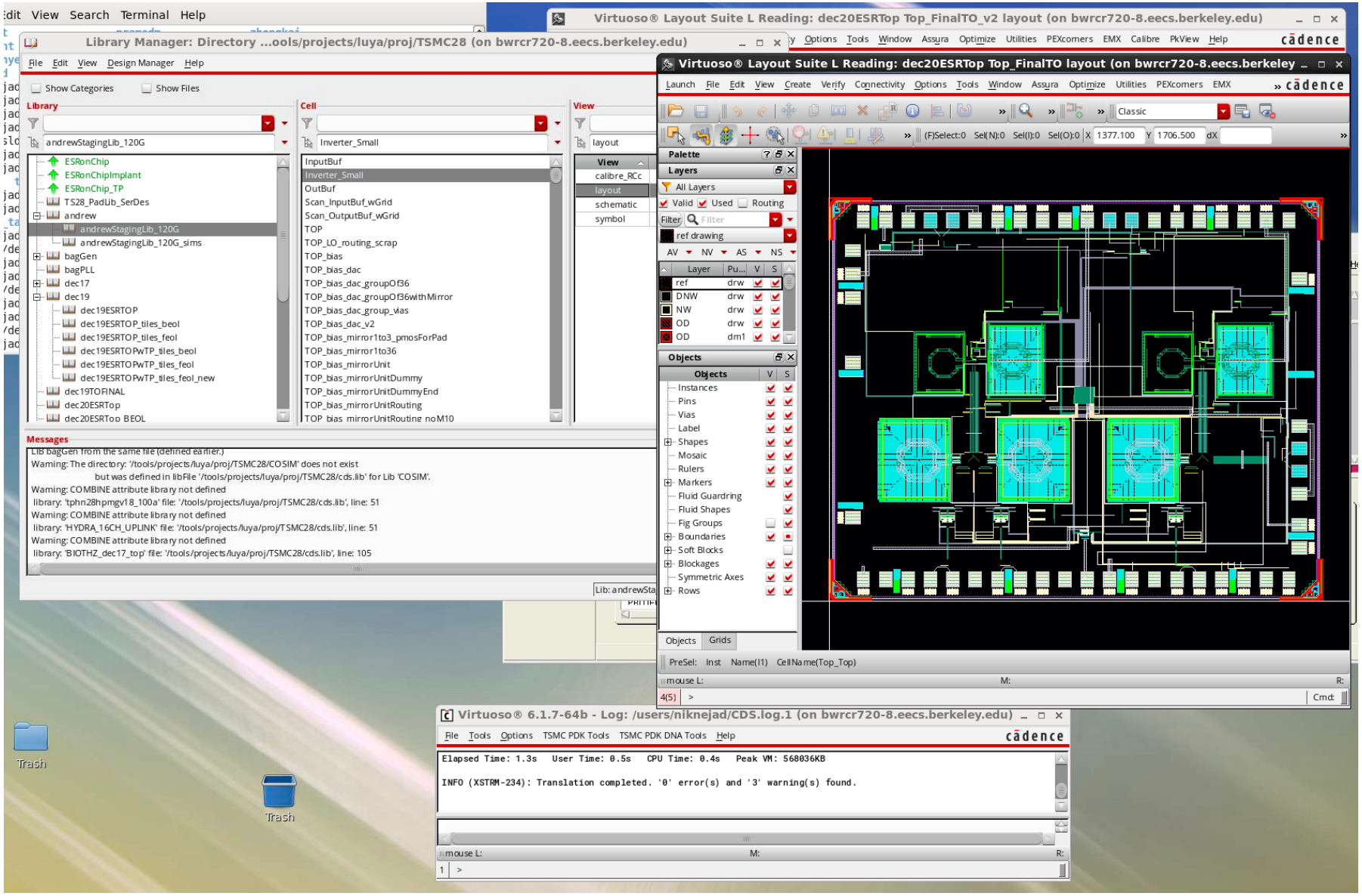




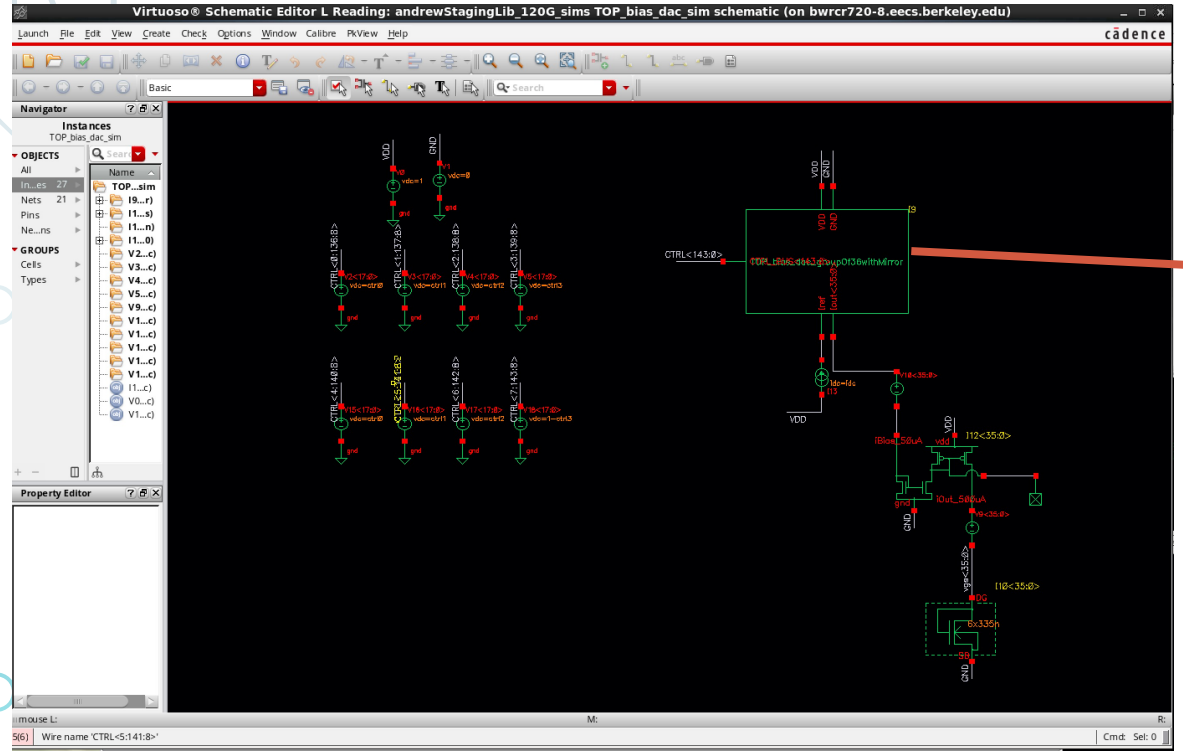
https://ucberkeleyee290c.github.io/sp21/

Layout Tutorial: Virtuoso Layout Environment

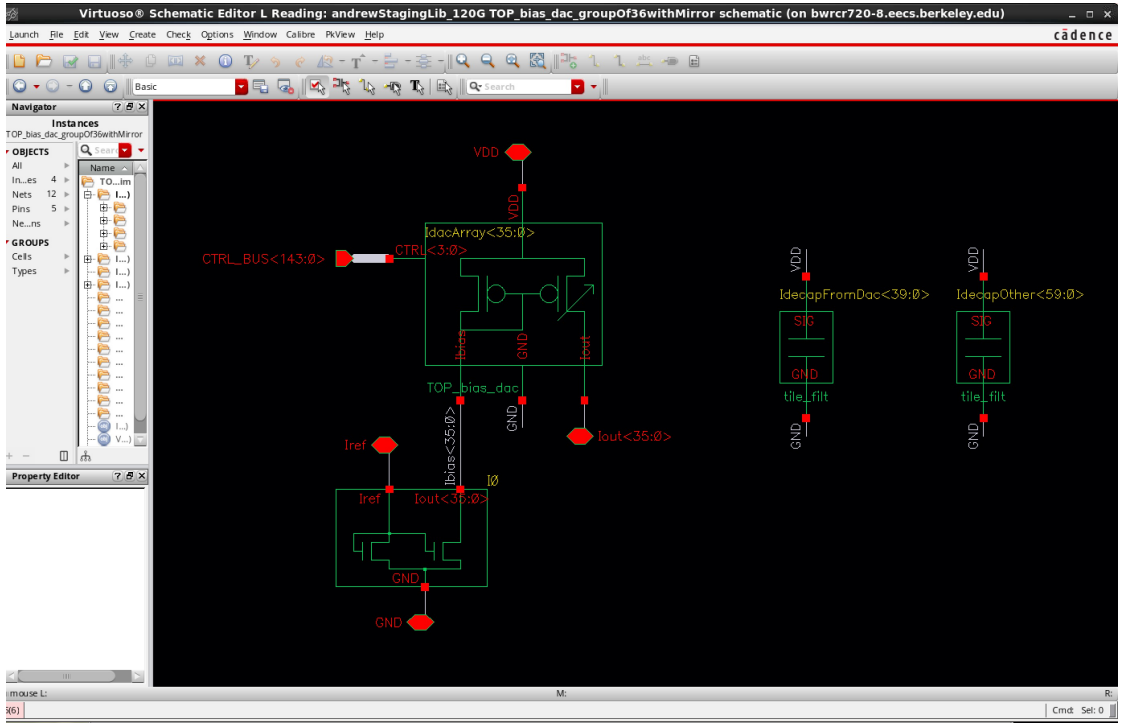
Cadence Environment



Testbench Example



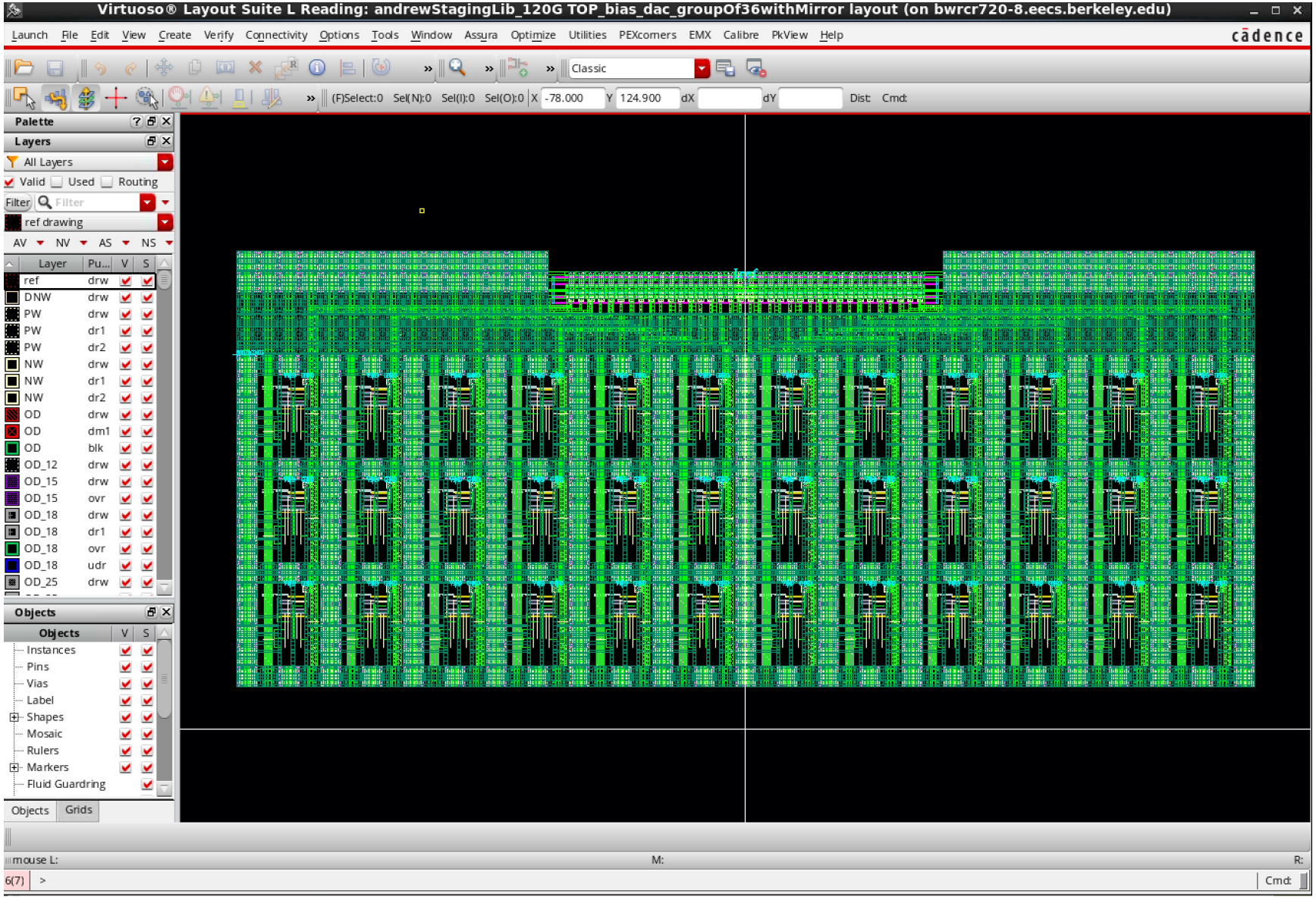
Schematic Cell



Schematic Cell

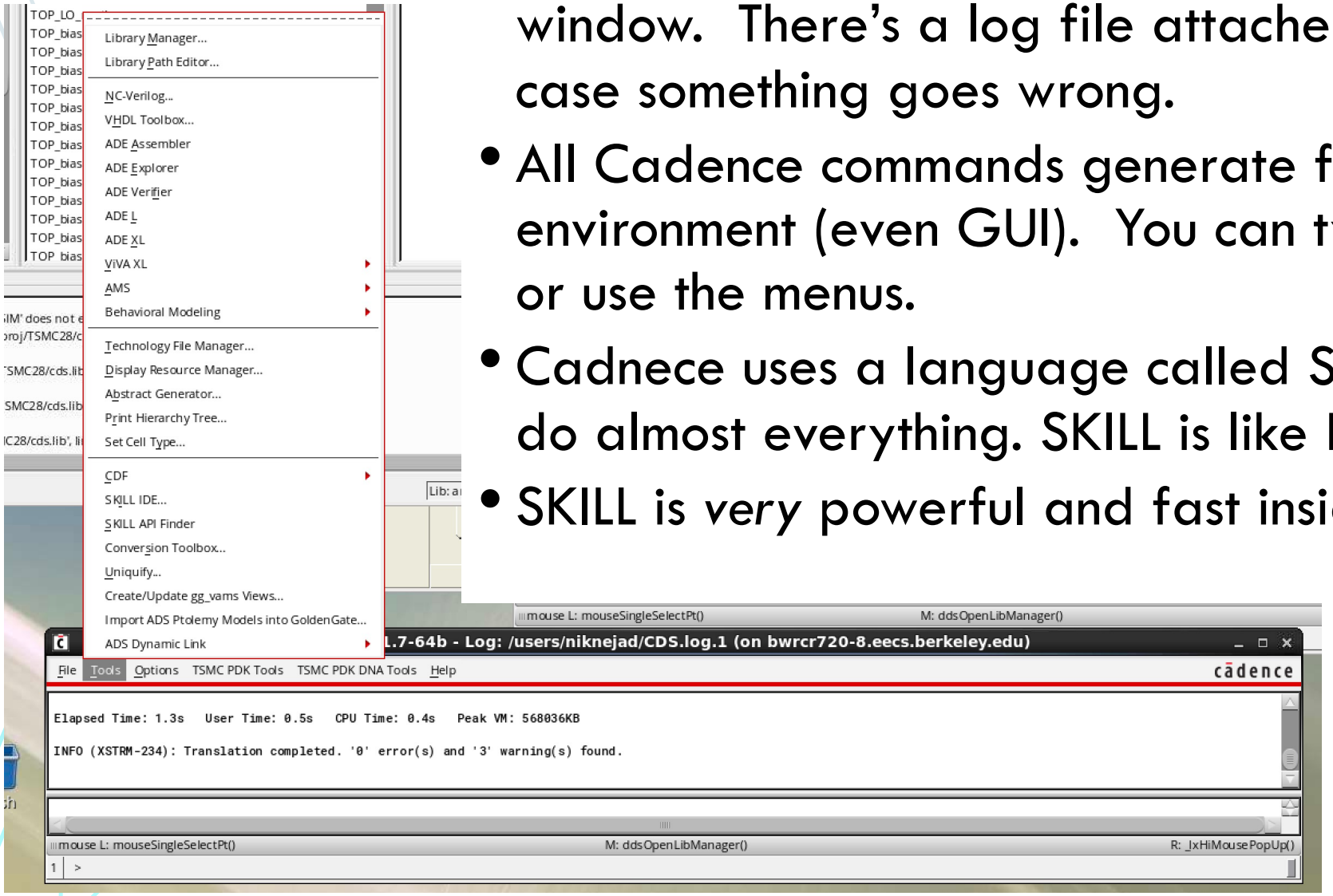
- Testbench can have "analog" components but the sub-cell should only contain technology library cells (or your custom cells)

Layout View …



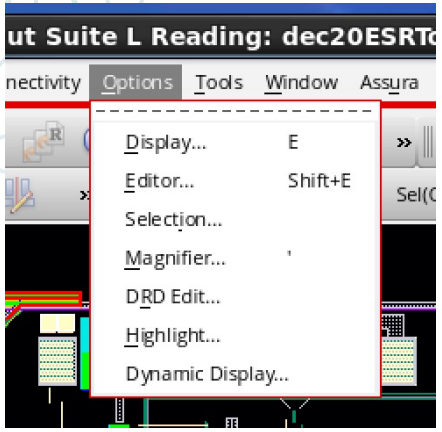
Layout Cell

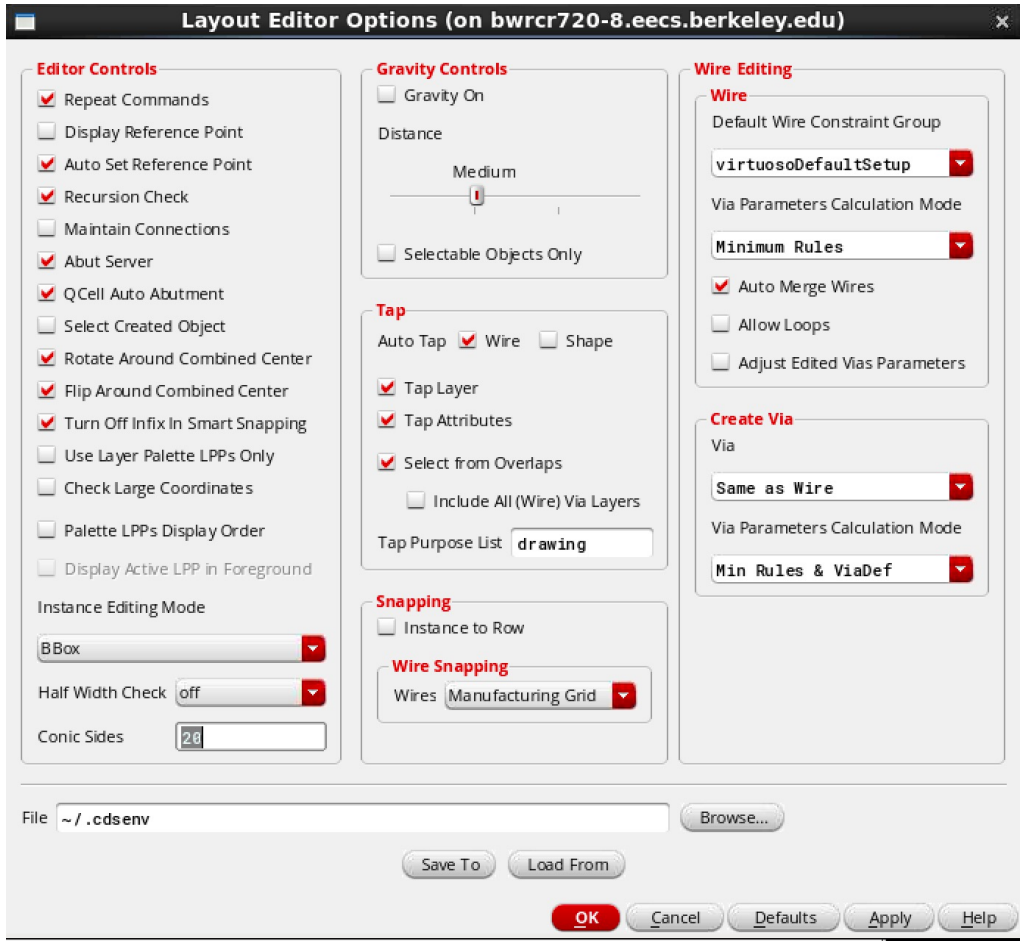
CIW Window

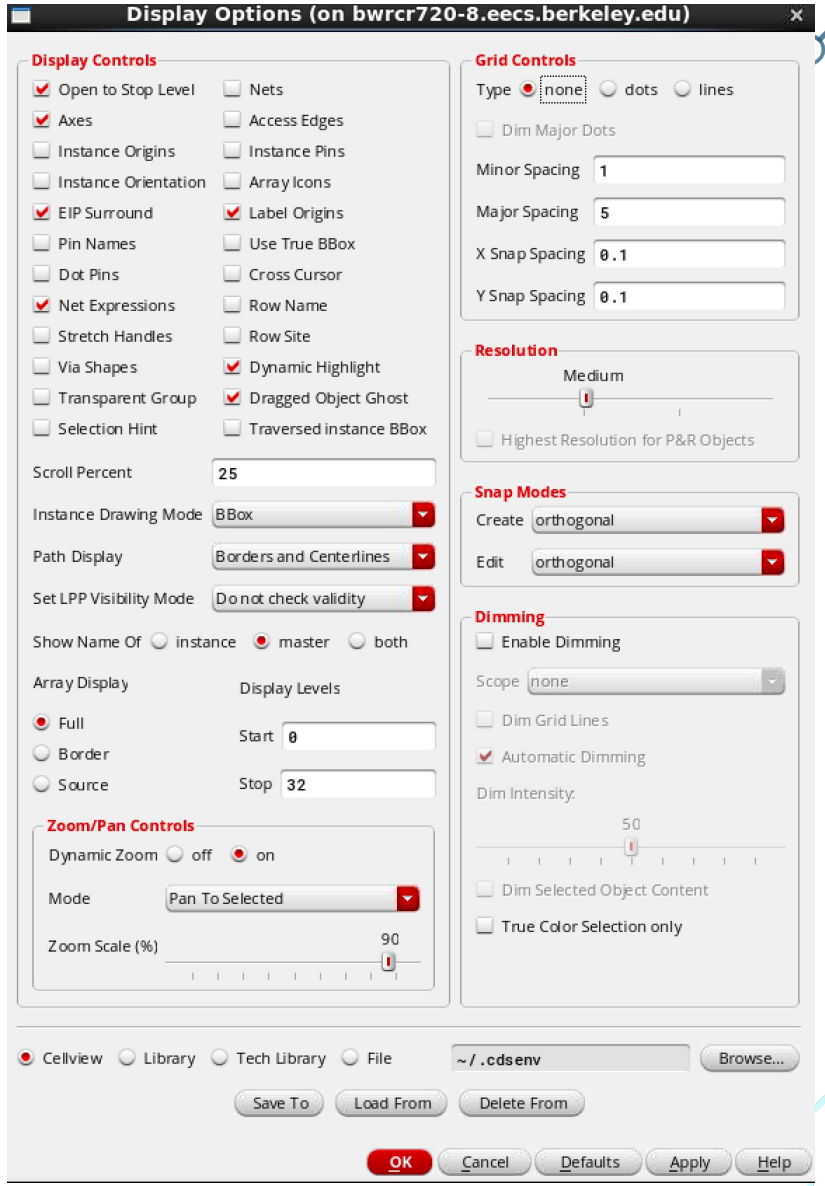


- Every Cadence session has this window. This is the main window. There's a log file attached to this window in case something goes wrong.
- All Cadence commands generate function calls inside this environment (even GUI). You can type commands here or use the menus.
- Cadnece uses a language called SKILL (and SKILL++) to do almost everything. SKILL is like LISP dressed up in C.
- SKILL is *very* powerful and fast inside Cadence

Environmental Setup

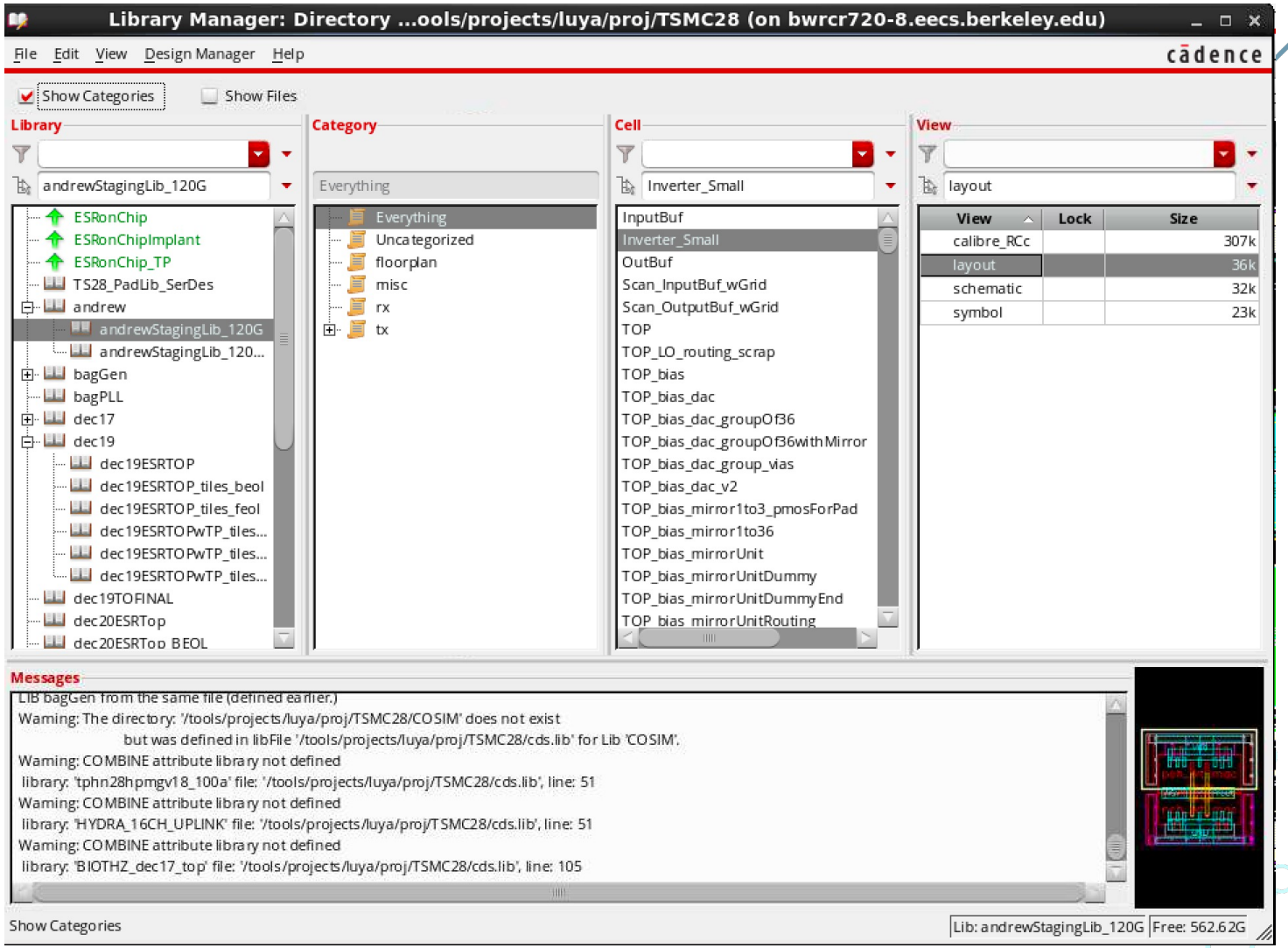






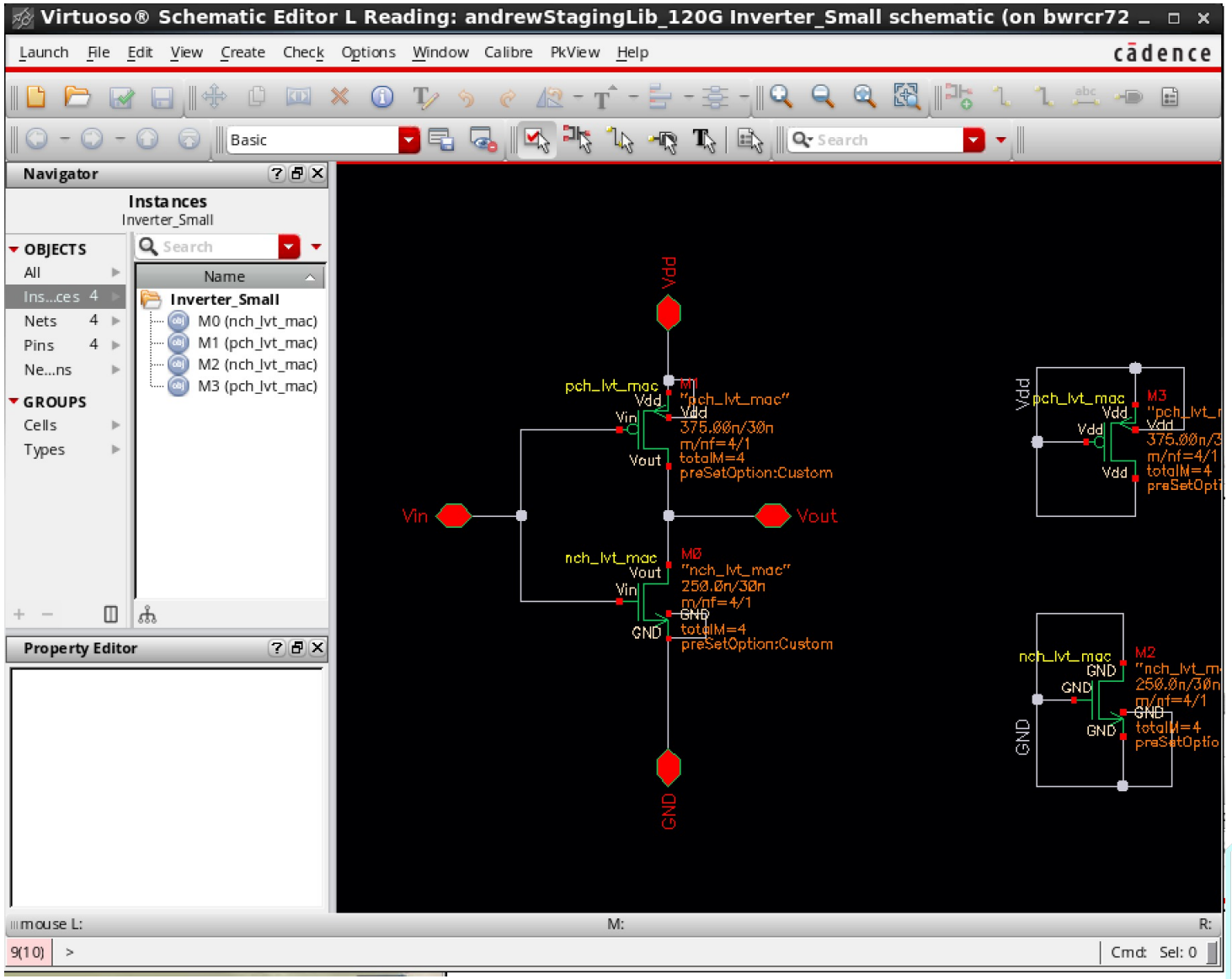
Library Manager Window

- Optional but very useful
- Each library is a database of cells.
- Each cell can have multiple views, such as schematic, layout, and symbol
- You can open/close and copy cells / libraries here
- Use the very powerful copy hierarchy command with caution



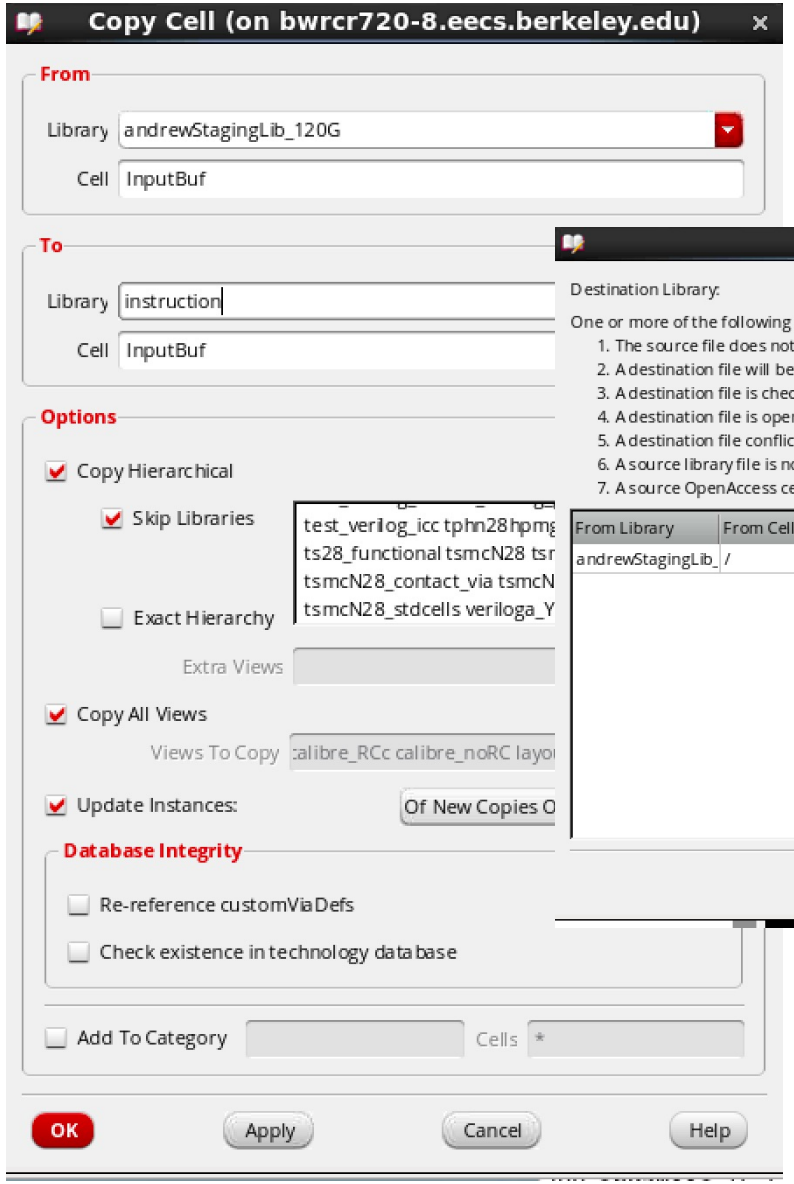
Schematic View

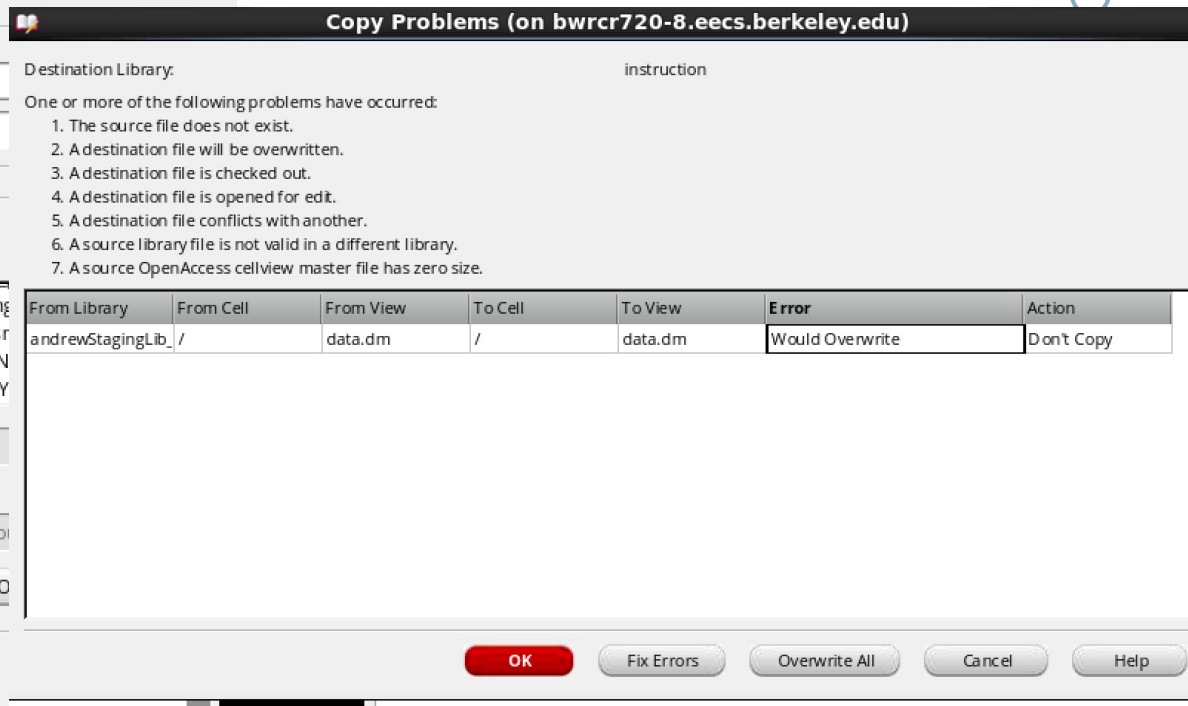
- The schematic view is obviously the schematic of a cell.
- Can view instances of a particular cell here and add instances.
- Learn powerful array techniques for creating schematics (arrays of nets, instances, etc)
- Note that “pins” are used to make connections to the outside. Schematics are very hierarchical in practice.
-



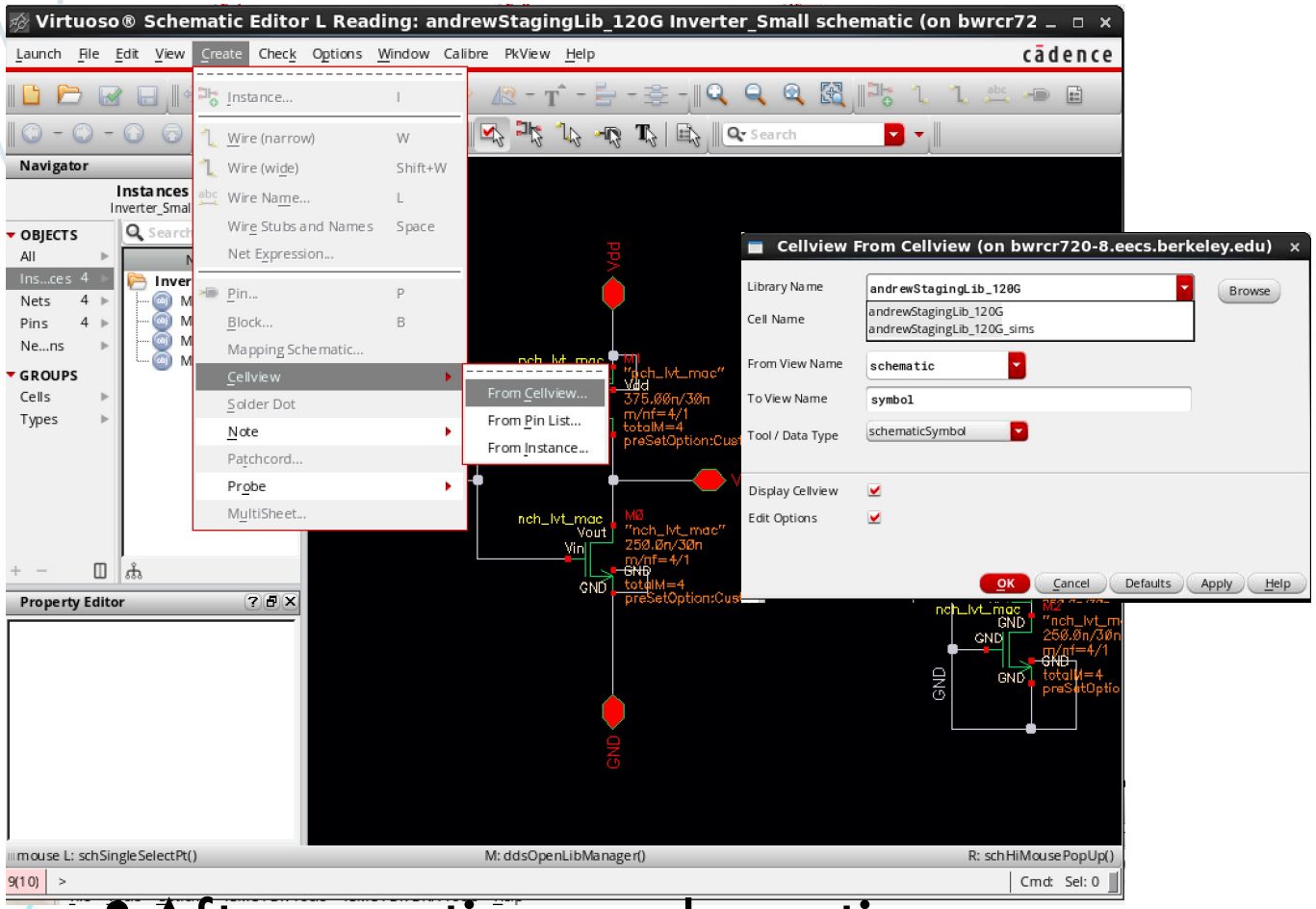
Copying a Hiearchy

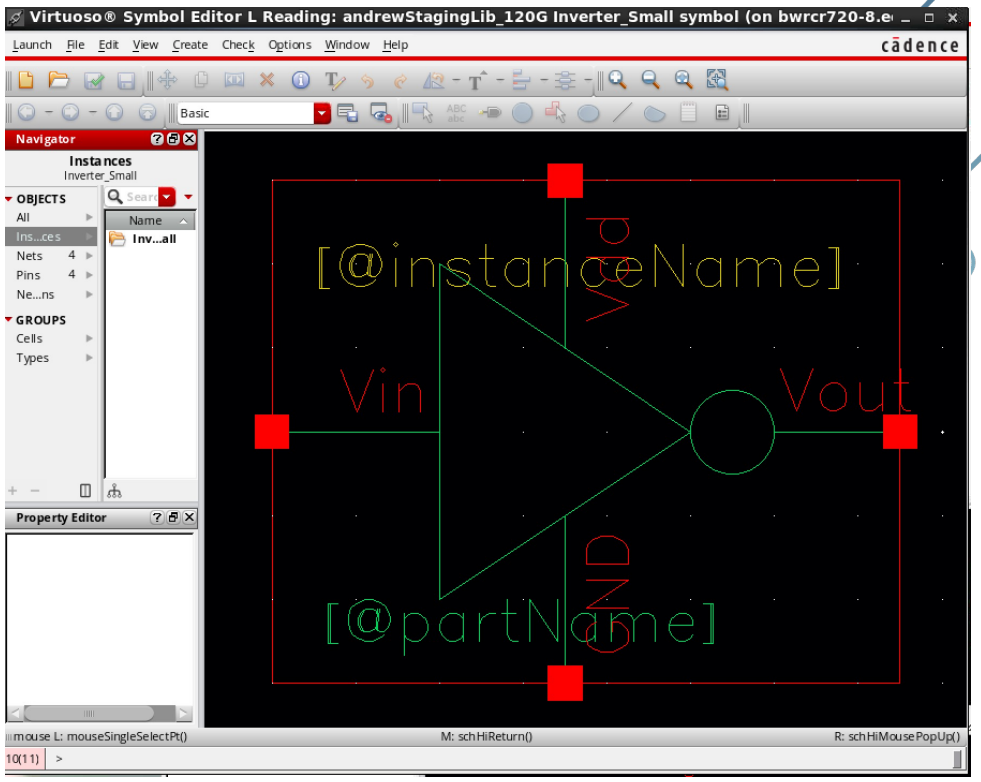
- Note that you should skip common libraries and avoid duplicating cells
- Update instances of new copies if you only want the new copies to point to the new files





Create a Symbol View

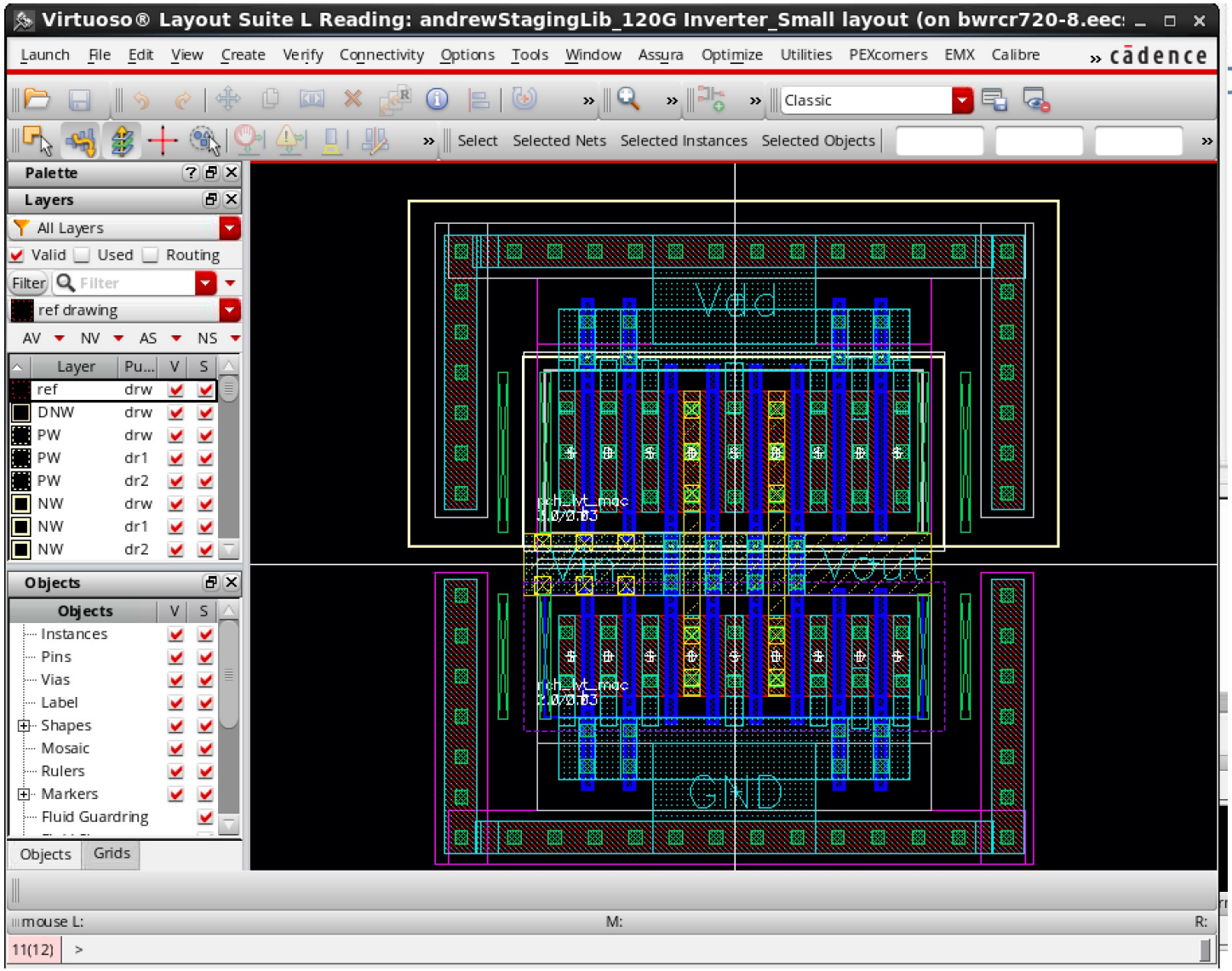




- After creating a schematic, you can generate a symbol view, and edit it as you see fit (make a useful graphic representation).
- If you modify a schematic, make sure you update the symbol (new pins or change in direction of pins)

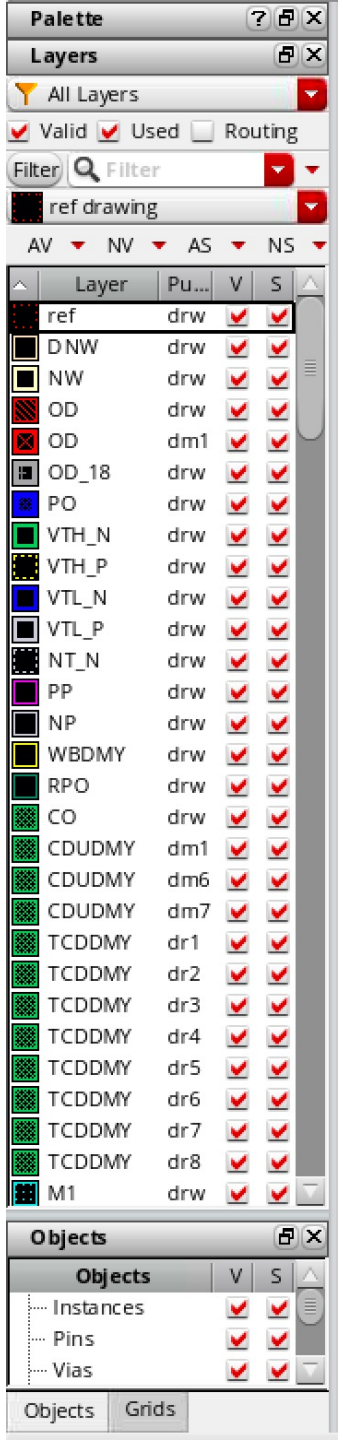
The Layout View

- We'll spend a lot of time talking about how to generate this layout. Don't worry, a lot of it is automated.



The Layers

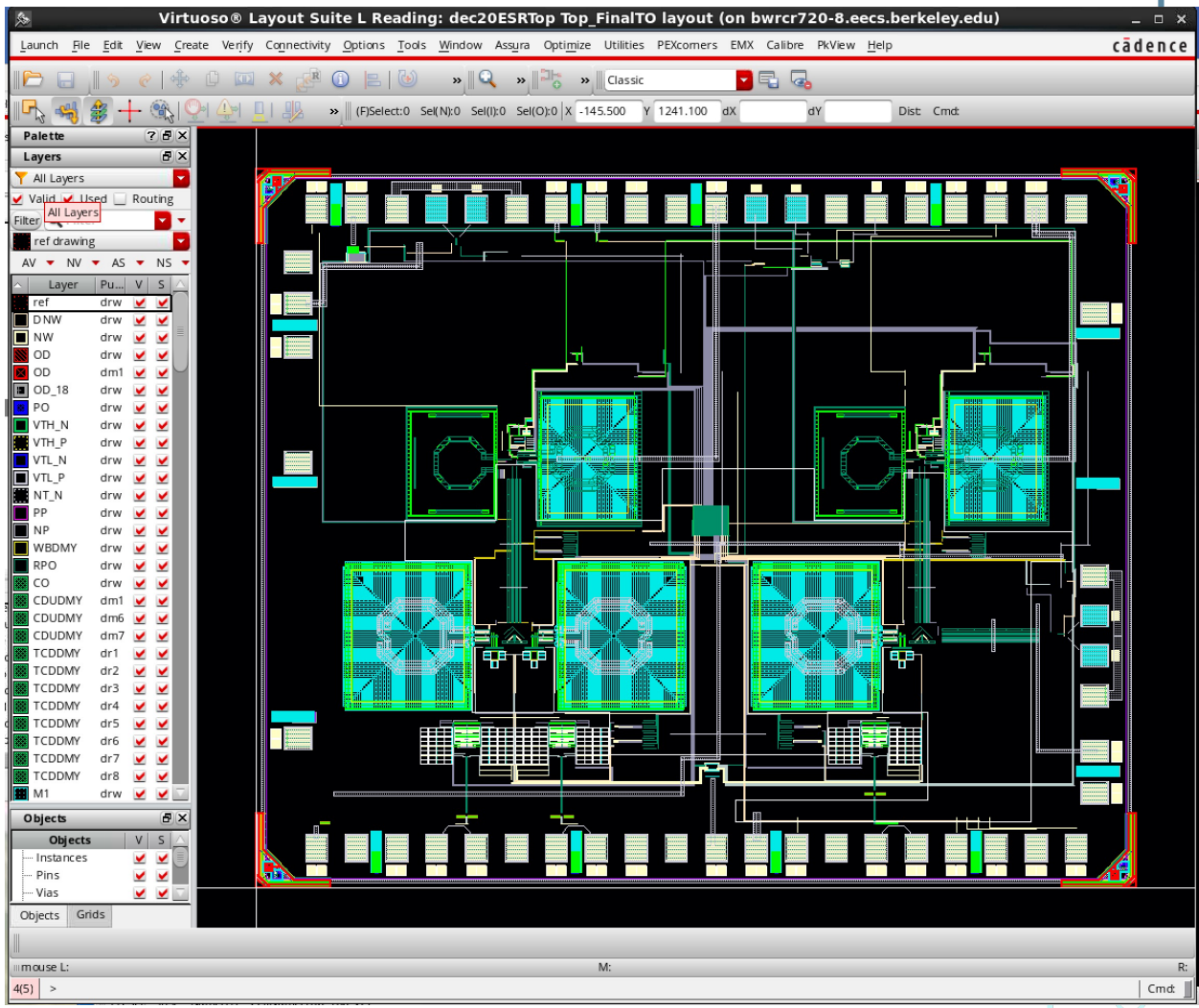
- A layout cell is essentially a database of polygons, mostly rectangles
- Each rectangle is on a particular layer, that has a very close connection with the fabrication steps of the process
- Diffusion layers, oxides, polysilicon, metal layers all have corresponding layers or are generated from a Boolean calculation of layers



- The layers "palette" is very useful and you should get to know it well
- Notice that you can also view "Used" or "Routing" layers to reduce the clutter
- Layers have multiple "purposes". Drawing layers are usually the ones that you manipulate

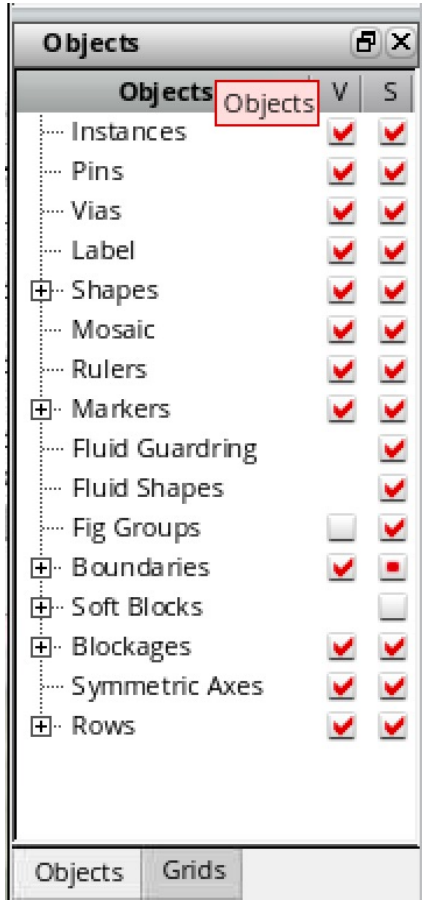
Be Careful What You Touch !

- Always open all cells “read only” and change “edit” permission when you really need it.
  - Accidentally clicking a cell and moving it by a fraction of a micron could result in a million DRC errors !
- Layout navigation aids help. See next slide

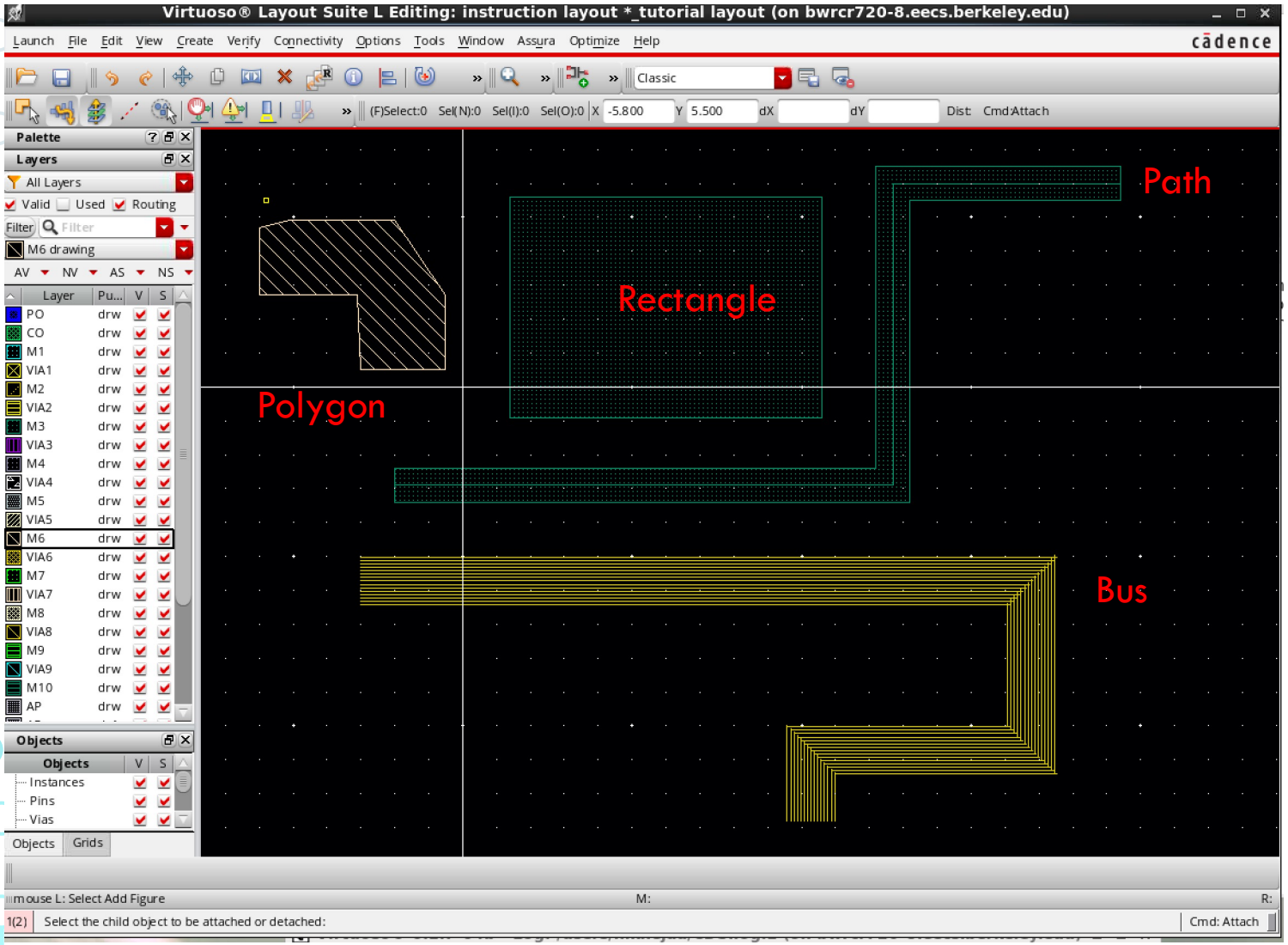


Layout Selection

- By default, anything you touch is selected and this is very dangerous.
- You can change the selectivity to only include:
  - Instances
  - Pins
  - Vias
  - Shapes
  - Mosaics
- If you're editing the layout and not making any changes to instances, you should only enable "shapes" and perhaps "mosaics"
- Mosaics are "tiles" of cells used to create patterns

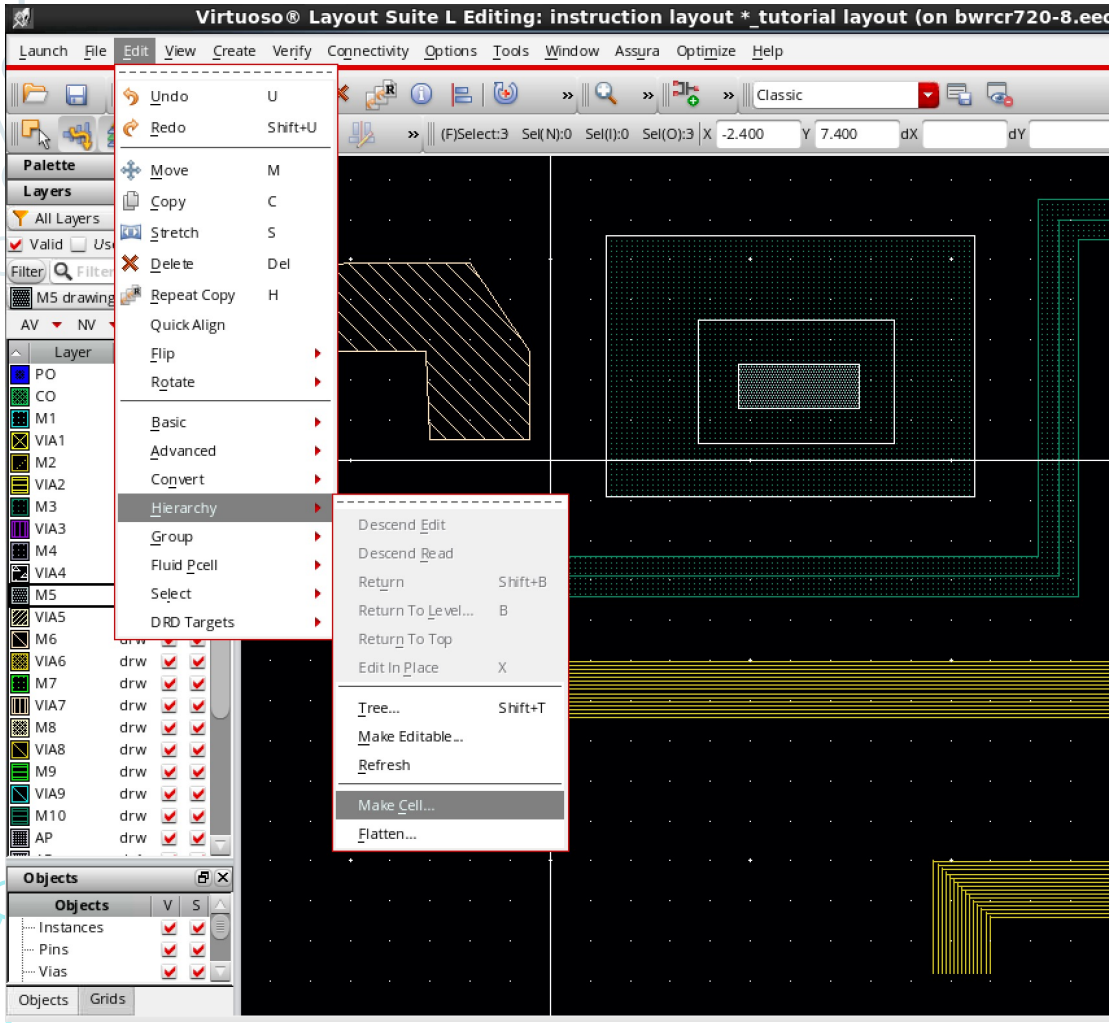


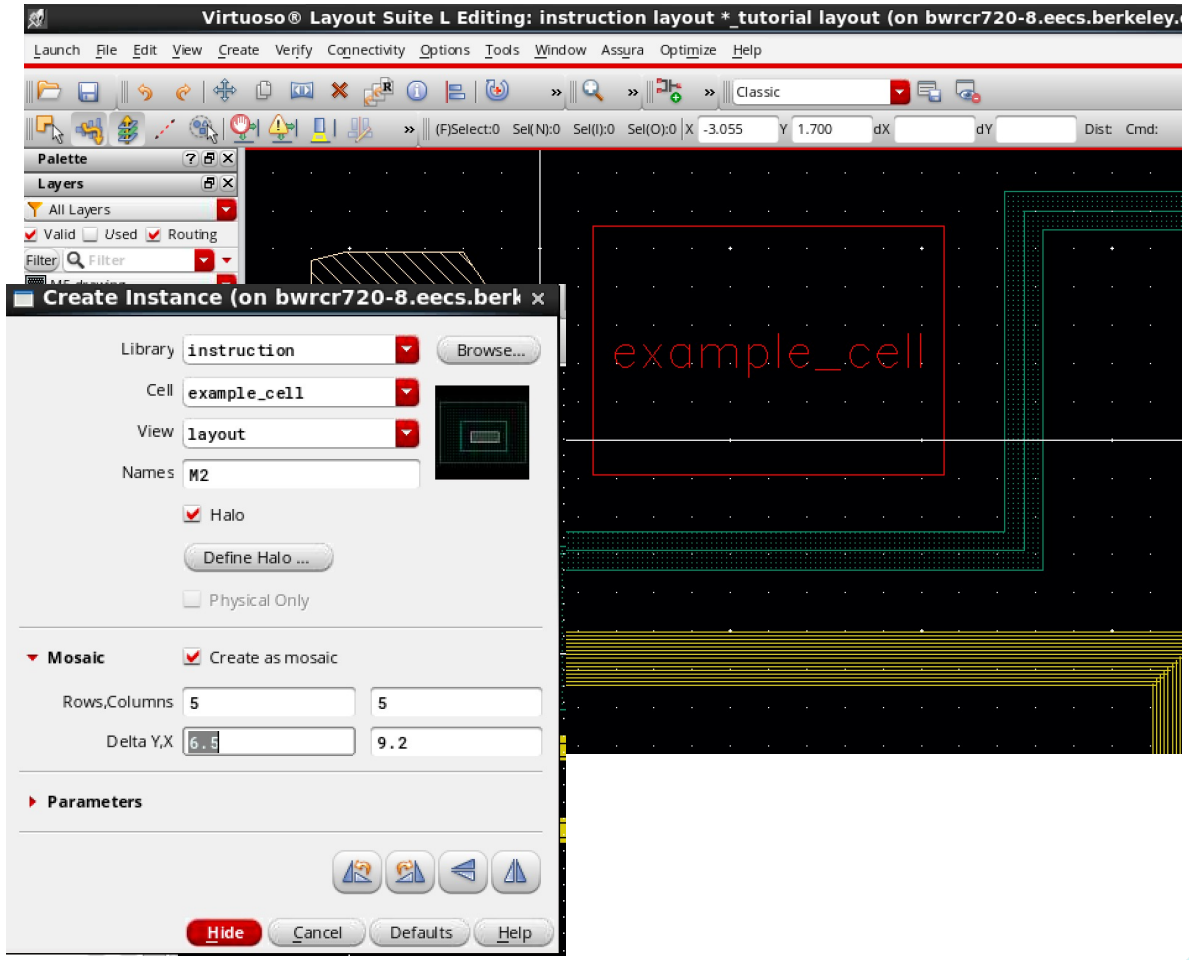
“Drawing” Your Layout



- Tyipcally you draw “Rectangles”, “Paths”, or “Polygons” (rare). Bus command is very useful and can be created from a list of pins.
- Copy (array), tile (mosaic) are common
- You can create “multi-part” paths to draw more complex structures, such as substrate contacts or a shielded wire
- Use hierarchy: Layout hierarchy does not need to match schematic. Many useful cells can be turned into cells, such as VDD/VSS connections

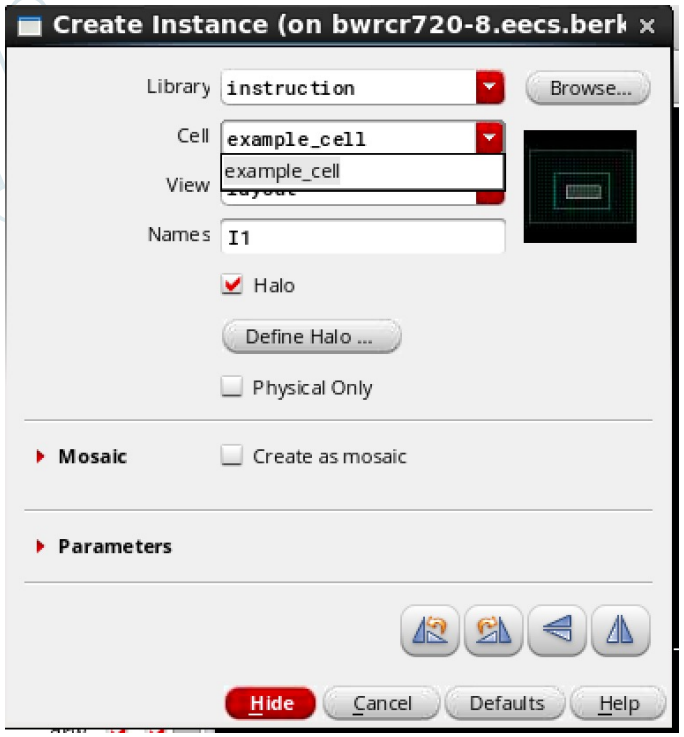
Creating a Cell on the Fly

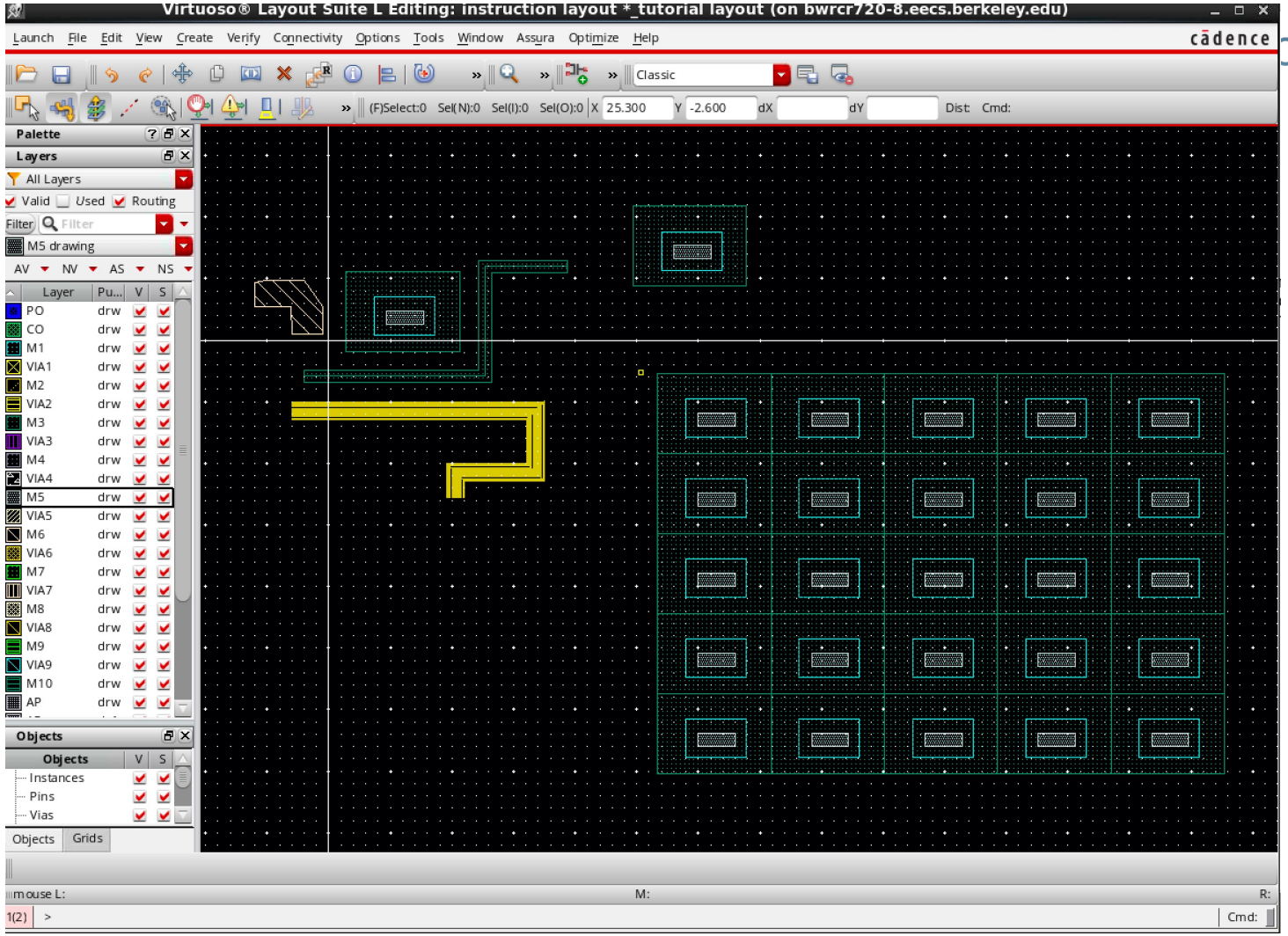




- You can view a cell "in place" and edit it one instance, all others will change simultaneously

Tiles

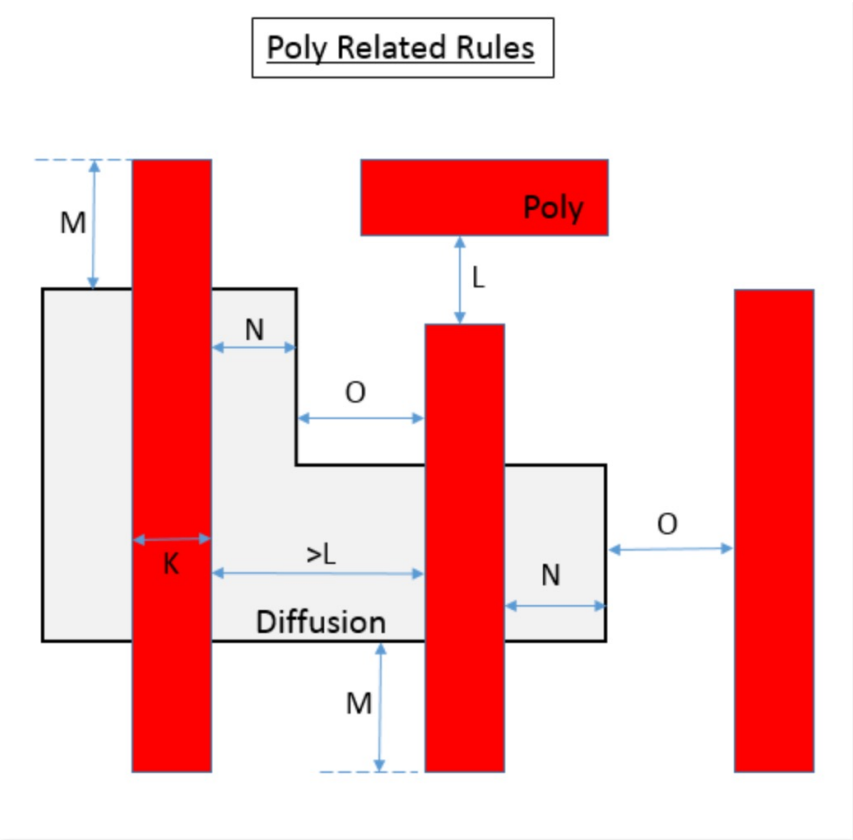




- Insert cell as a tile is very convenient for adding an array of identical cells

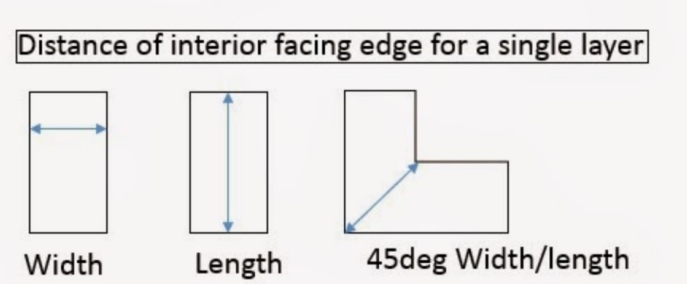
Design Rules

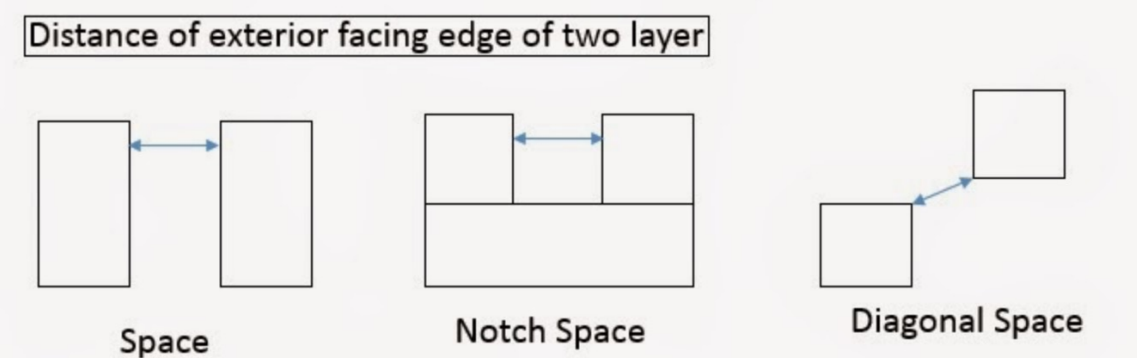
- Design rules are in place based on manufacturing limits
- If you do not meet all the design rules, the manufacturer (Intel, TSMC, others) will usually refuse to fabricate your chip
- Each layer has its own set of rules

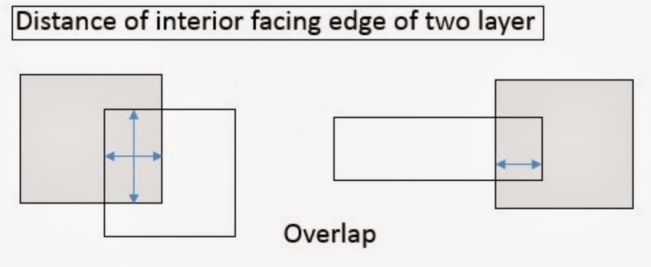


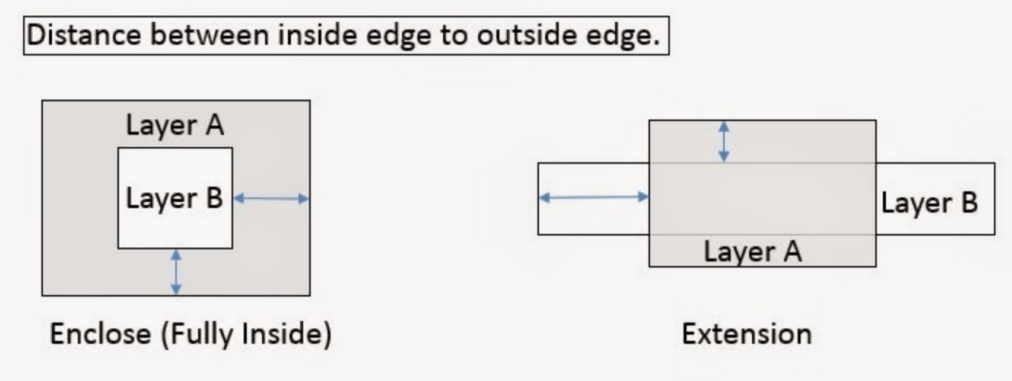
Layer	Description	Label	Rule
Contact	Width (Minimum = Maximum)	P	=W.C
	Minimum Space	Q	>=S.C
	Min Space (When Contacts are on different Nets)	R	>=S1.C
	(Contact over Diff) minimum Space to Poly	S	>=S2.C
	(Contact over Poly)minimum Space to Diff	T	<=S3.C
	Enclosure by Diff	U	>=E.C

DRC Concepts

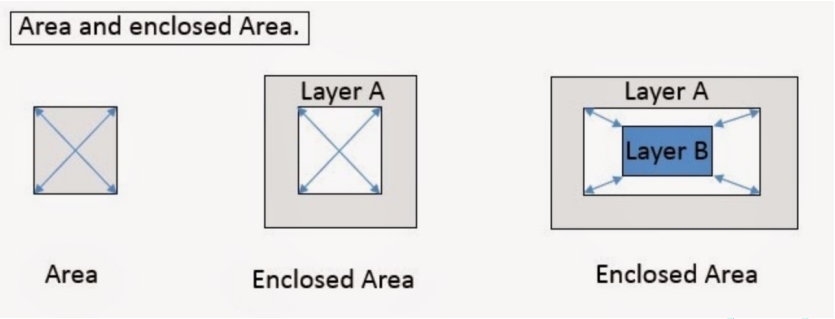








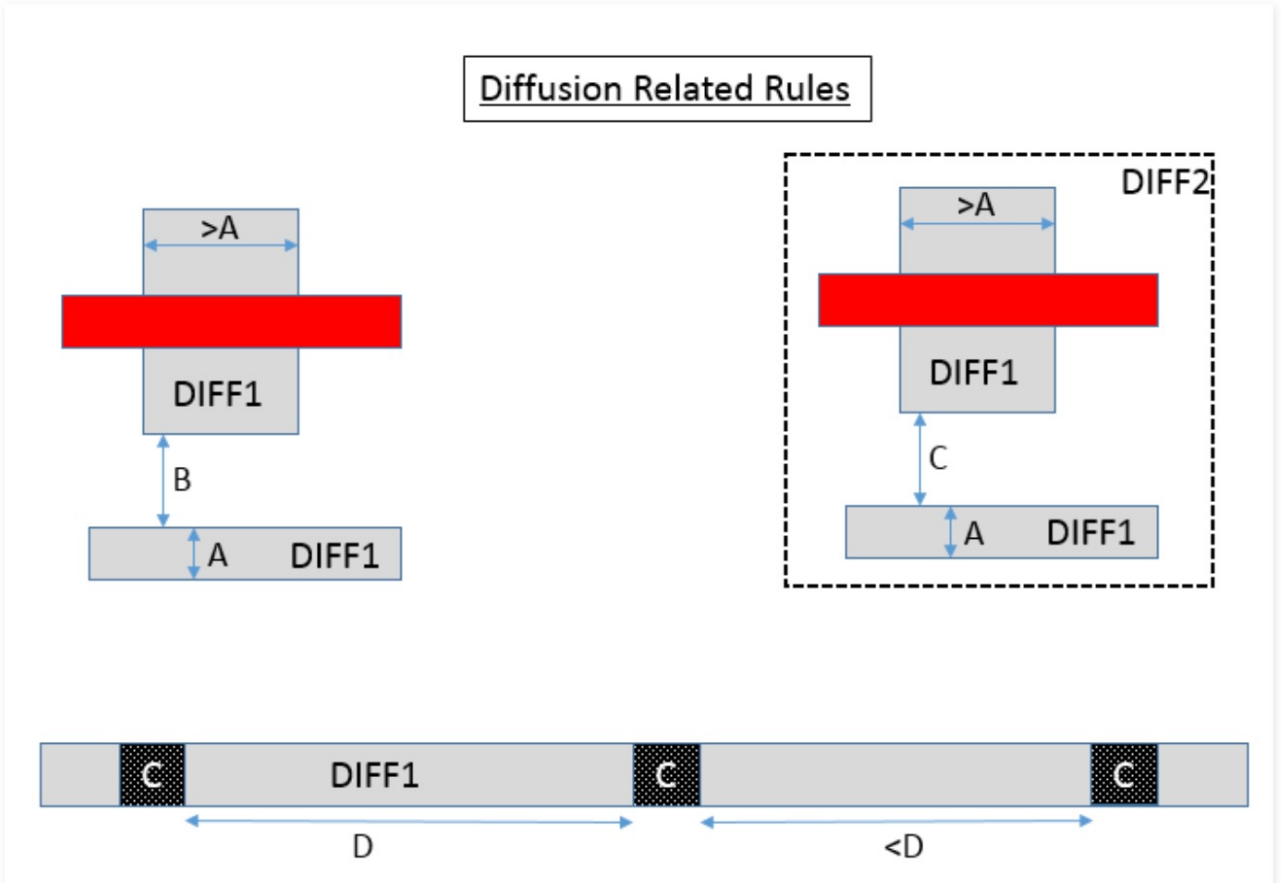
- The best way to learn the rules is to do some actual layouts and use the tools to tell you what mistakes you're making !



http://www.vlsi-expert.com/2014/12/design-rule-check.html

DRC: Diffusion

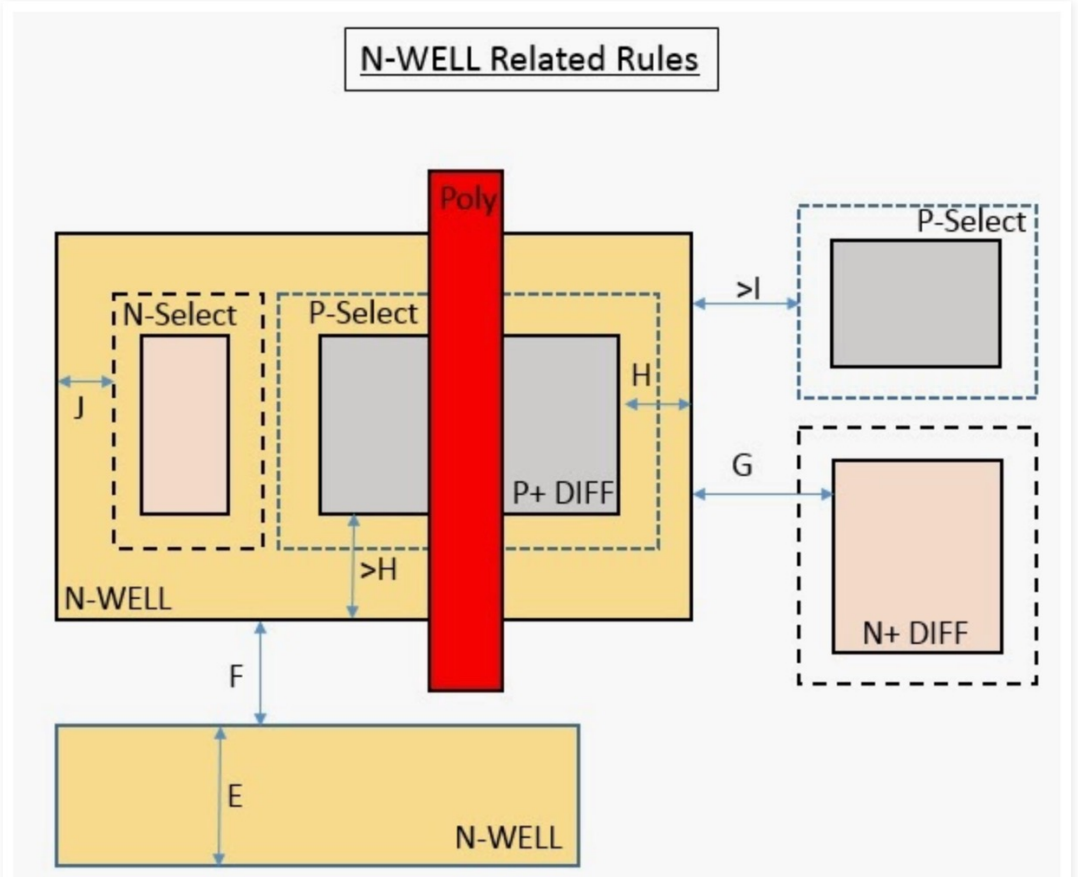
Layer	Description	Label	Rule
Diffusion	Min Width	A	>=W.D
	Min Space	B	>=S.D
	Min Space between 2 DIFF1 with in DIFF2	C	>=S1.D
	Maximum DIFF length between 2 contacts	D	<=L.D
	DIFF must be fully covered by N/P select		



http://www.vlsi-expert.com/2014/12/design-rule-check.html

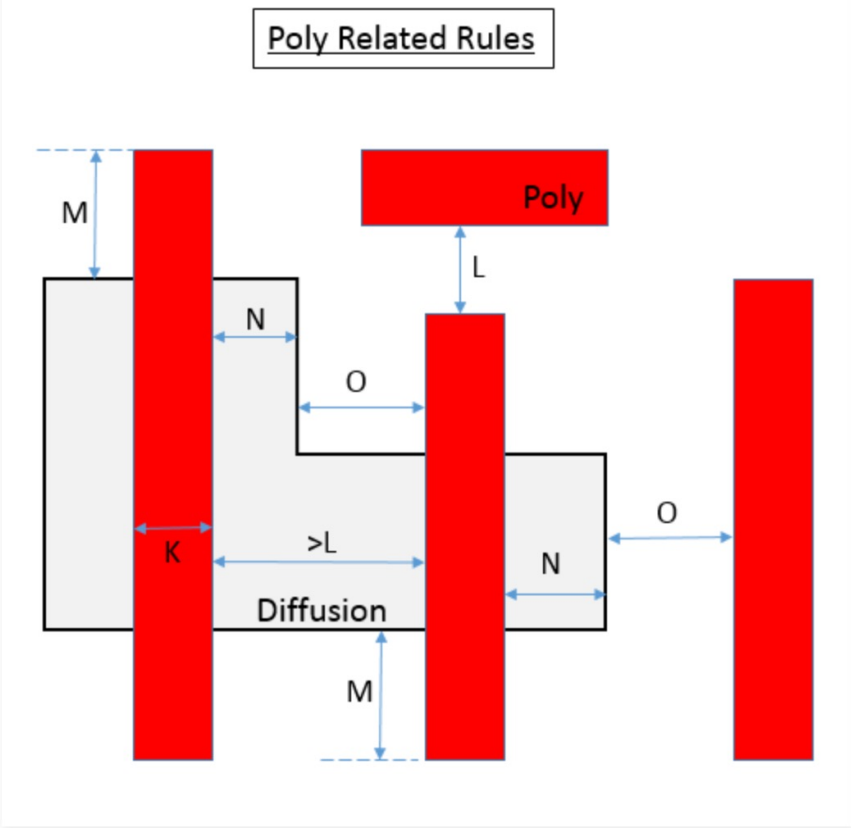
DRC: NWELL

Layer	Description	Label	Rule
N-Well	Min Width	E	>=W.NW
	Min Space	F	>=S.NW
	Min Space to N+ Diffusion/Active	G	>=S1.NW
	Min Enclosure of P+ Diffusion / Active	H	<=E.NW
	Min Space to P Select	I	>=S2.NW
	Min Enclosure of N select	J	>=E1.NW



http://www.vlsi-expert.com/2014/12/design-rule-check.html

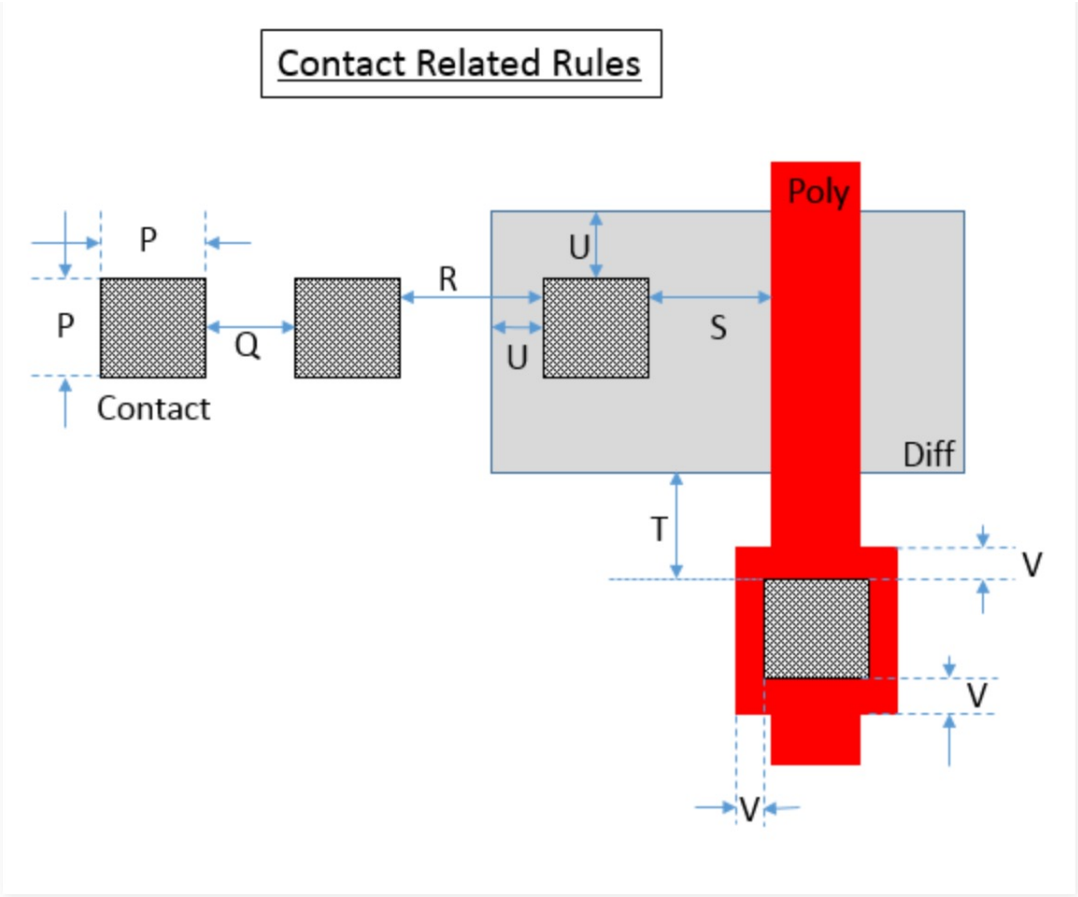
DRC: Poly



Layer	Description	Label	Rule
Contact	Width (Minimum = Maximum)	P	=W.C
	Minimum Space	Q	>=S.C
	Min Space (When Contacts are on different Nets)	R	>=S1.C
	(Contact over Diff) minimum Space to Poly	S	>=S2.C
	(Contact over Poly)minimum Space to Diff	T	<=S3.C
	Enclosure by Diff	U	>=E.C
	Enclosure By Poly	V	>=E1.C

http://www.vlsi-expert.com/2014/12/design-rule-check.html

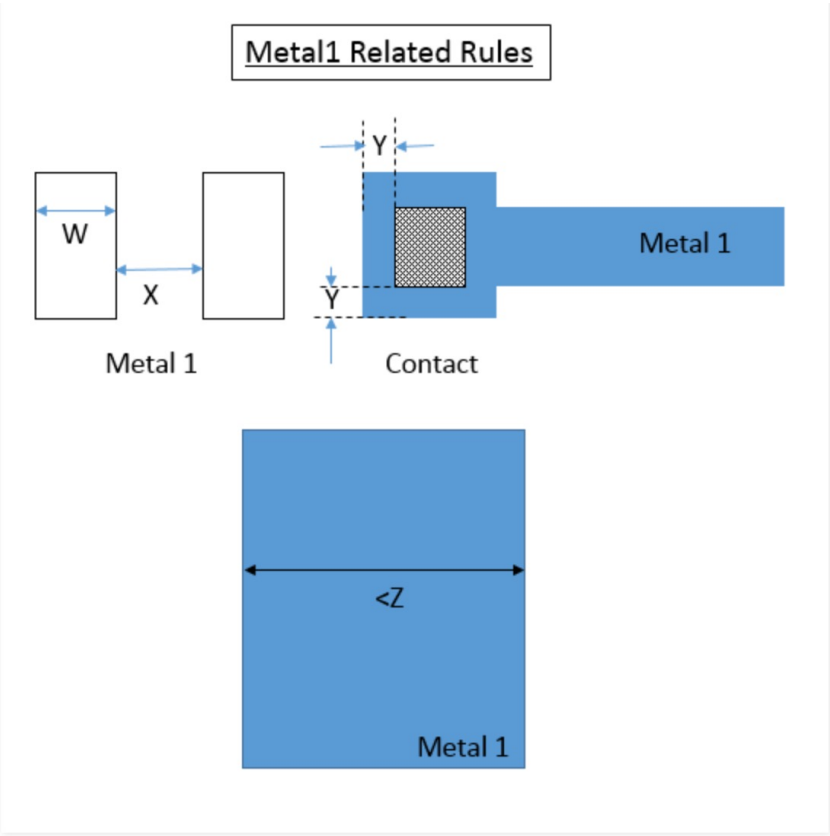
DRC: Contact



Layer	Description	Label	Rule
Metal 1	Min Width	W	>=W.M
	Minimum Spacing	X	>=S.M
	Enclosure of Contact	Y	>=E.M
	Maximum Width	Z	<=W1.M

http://www.vlsi-expert.com/2014/12/design-rule-check.html

DRC: Metal



- Upper (thick) layers have their own distict rules

http://www.vlsi-expert.com/2014/12/design-rule-check.html

Calibre Deck

- It's very rare that you'll need to edit the Calibre DRC deck.
- This is created by the manufacturer.
- In a rare circumstance where you simply cannot understand the documentation, you can try to figure out how to solve an issue by looking here:

```
NSTP          = NPOD AND NONWR          // NWEL tap diffusion
NACT          = NPOD NOT NWEL           // NMOS device active diffusion
PACT          = PPOD AND NWEL           // PMOS device active diffusion
NACT2         = NACT INTERACT OD2
PACT2         = PACT INTERACT OD2
PSTP          = PPOD NOT NWEL           // Substrate (pwell) tap diffusion
DACT          = NACT OR PACT            // NMOS/PMOS device active diffusion
DSTP          = NSTP OR PSTP

GATE          = POLY AND OD             // Gate regions for NMOS and PMOS
GATEi         = POi AND ODi             // Gate regions for NMOS and PMOS
SD            = (DACT ENCLOSE GATE) NOT GATE  // Source, drain areas
FPO1          = POLY NOT OD             // Field poly
HV_GATE       = GATE AND OD2
LV_GATE       = GATE NOT OD2
GATE_NP       = GATE AND NP
GATE_PP       = GATE AND PP
GATE_W        = POLY COIN INSIDE EDGE GATE      // Gate width
GATE_L        = GATE NOT TOUCH EDGE GATE_W
GATEN_W       = GATE_W INSIDE EDGE NP
GATEP_W       = GATE_W INSIDE EDGE PP
HV_GATE_W     = GATE_W INSIDE EDGE OD2         // 2.5V/3.3V/1.8V MOS gates
LV_GATE_W     = GATE_W NOT INSIDE EDGE OD2     // 1.0V MOS gates
HV_GATE_L     = GATE_L INSIDE EDGE OD2         // 2.5V/1.8V MOS gates
LV_GATE_L     = GATE_L NOT INSIDE EDGE OD2
15V_GATE_W    = HV_GATE_W INSIDE EDGE OD15
18V_GATE_W    = HV_GATE_W INSIDE EDGE OD18
25V_GATE_W    = HV_GATE_W INSIDE EDGE OD25
33V_GATE_W    = HV_GATE_W INSIDE EDGE OD33


SR_GATE       = SRDPO AND OD
SR_GATE_W     = SRDPO COIN INSIDE EDGE SR_GATE
SR_GATE_L     = SR_GATE NOT TOUCH EDGE SR_GATE_W
SR_HV_GATE    = SR_GATE AND OD2
LV_SR_GATE = SR_GATE NOT OD2
WLD_LV_GATE = LV_GATE NOT OUTSIDE SRAMDMY_WLD
```

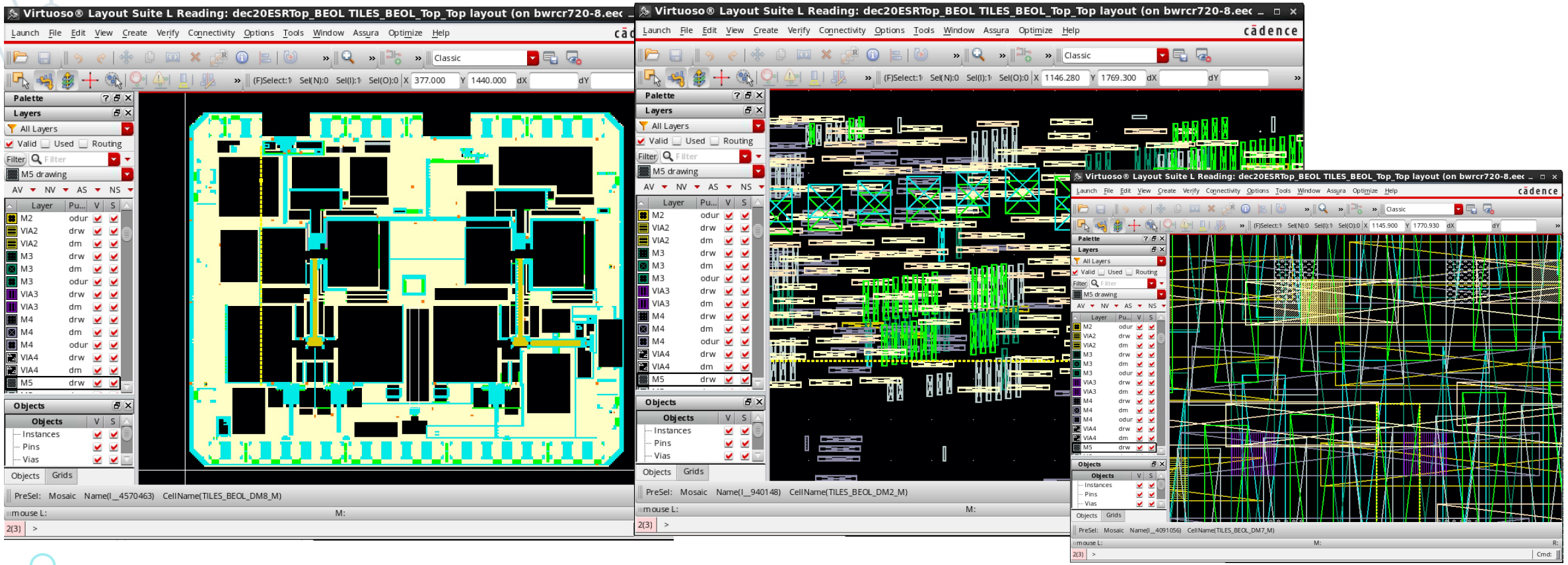
Design Rules for Manufacturing

- While the normal design rules are the best a manufacturer can do in high volume, you'll getter better yield if you follow a relaxed set of rules.
- For example, you can always use minimize sized diffusion regions, and this will minimize the area of your layouts, but it makes routing more complex. Also, you can use minimum width metals for local routing, but for longer range the width will vary due to roughness.
  - Router at 200nm width rather than 50nm !
- Simply relaxing the rules and making everything (except critical dimensions such as channel length) slightly bigger makes life easier and the extra space can be hand for layout changes (for example leave extra room between two wells rather than going all the way to the minimum)

Rules of Thumb

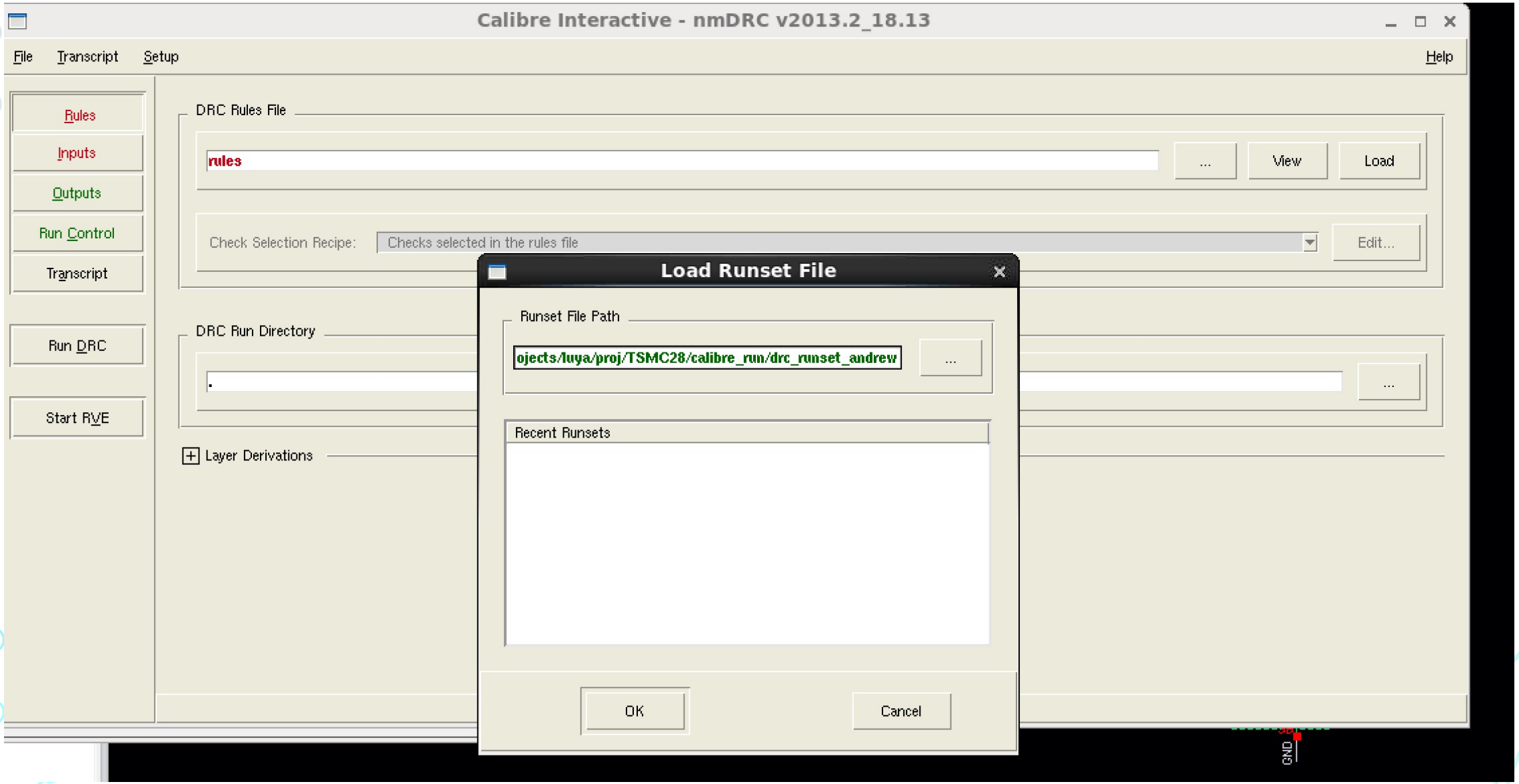
- Don't forget to put copious amounts of supply decoupling / bypass capacitors on your supplies.
- Use a tile cell that contains MOS + metal capacitors and just put it everywhere !
- Put a lot of substrate contacts near your devices.
- In digital high-performance cells, the supply capacitance should be 10X the size of the logic size
- Use two vias instead of one via so make sure you always make good connections.
- Route long lines with non-minimal metal widths.

Dummy Metals and Filling

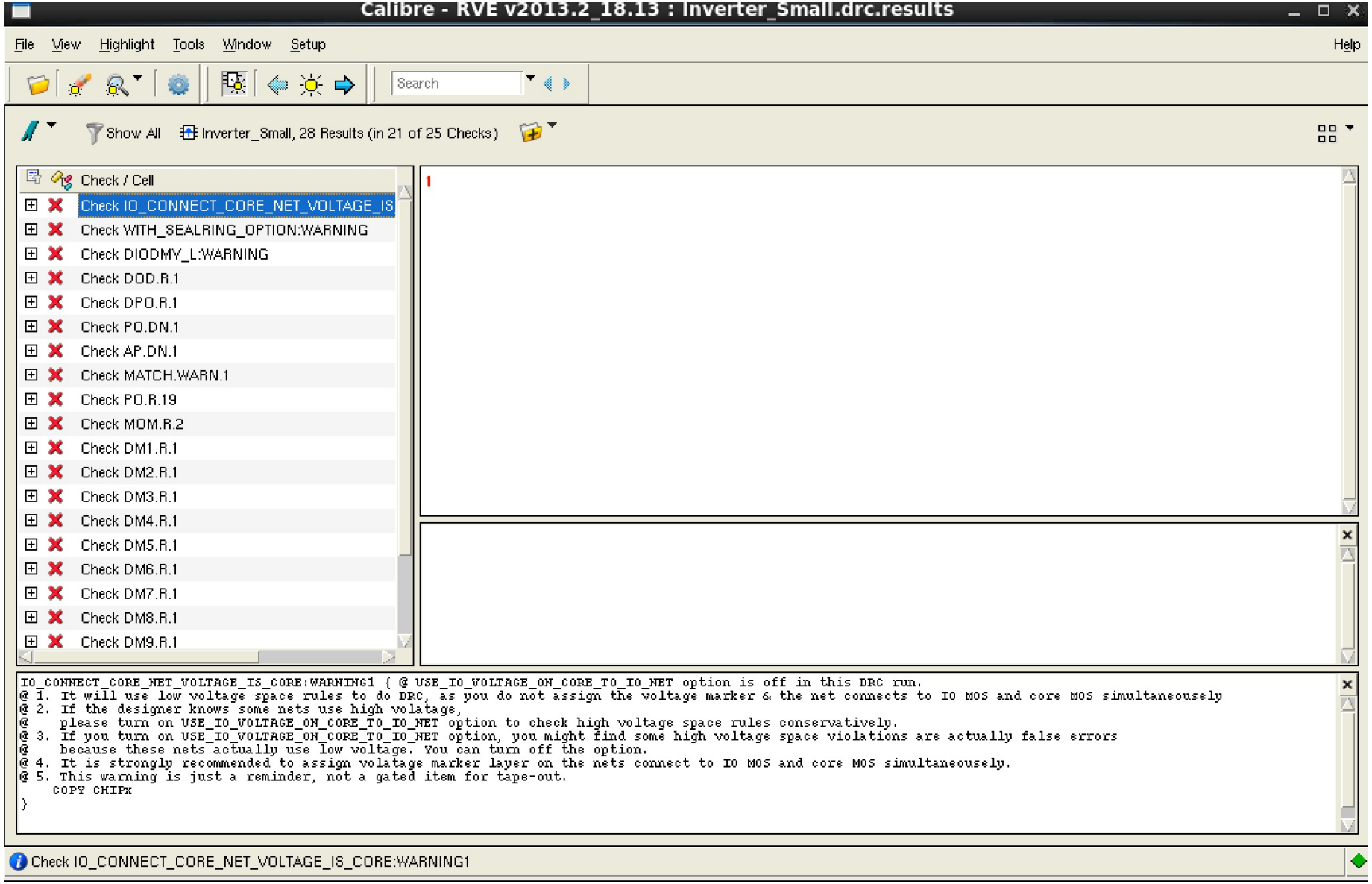


- After the layout is complete, the last step is to “dummy” fill the layout
- Scripted: Adds dummy metals, OD, poly, etc to keep density uniform
- Density rules have to be met both globally and locally (sliding window)

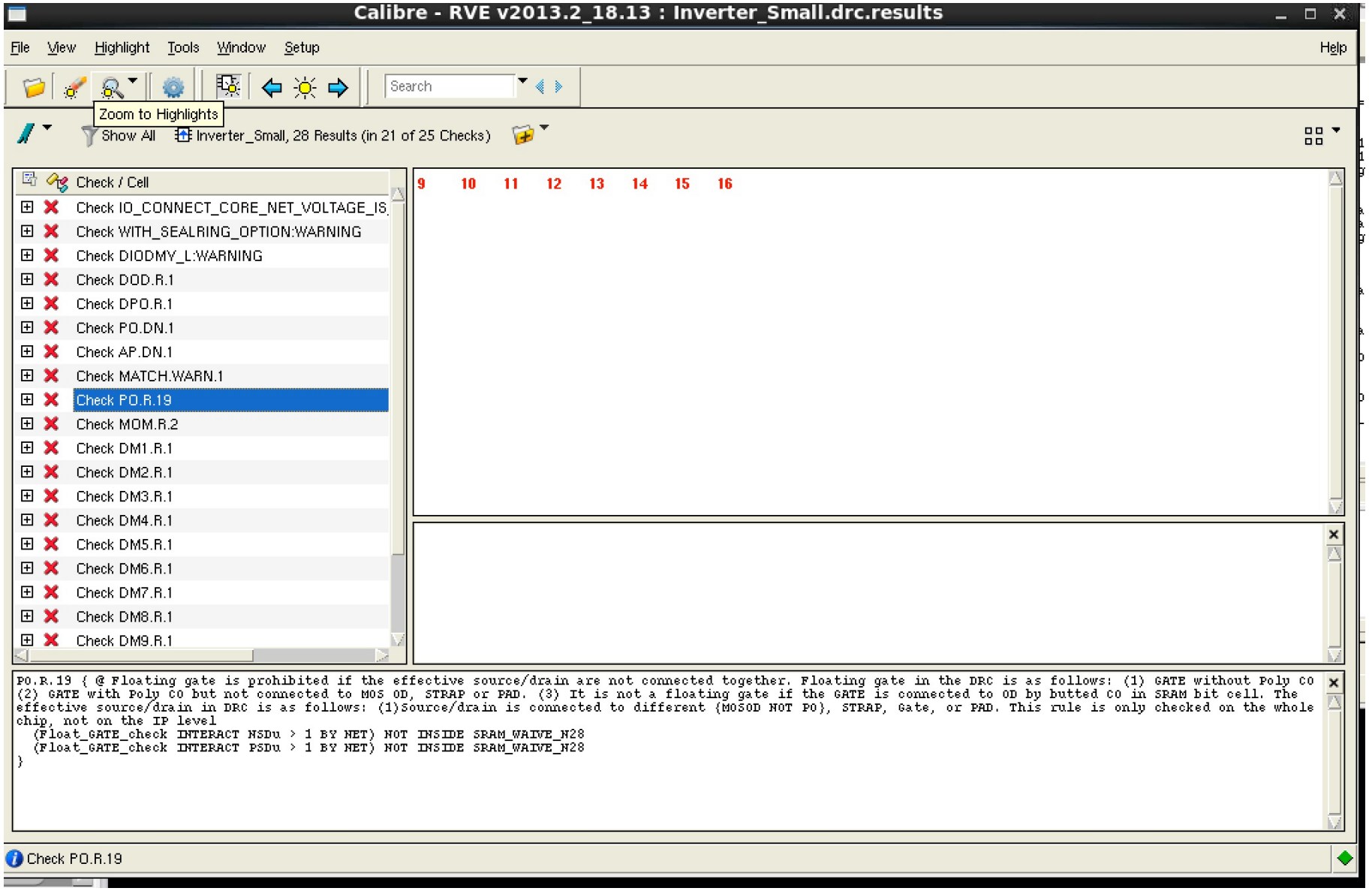
Running DRC


Calibre Interactive - nmDRC v2013.2_18.13
File
Transcript
Setup
Help
Rules
Inputs
Outputs
Run Control
Transcript
Run DRC
Start RVE
DRC Rules File
rules
...
View
Load
Check Selection Recipe:
Checks selected in the rules file
Edit...
DRC Run Directory
.
Layer Derivations
Load Runset File
Runset File Path
ojects/luya/proj/TSMC28/calibre_run/drc_runset_andrew
Recent Runsets
OK
Cancel
GND

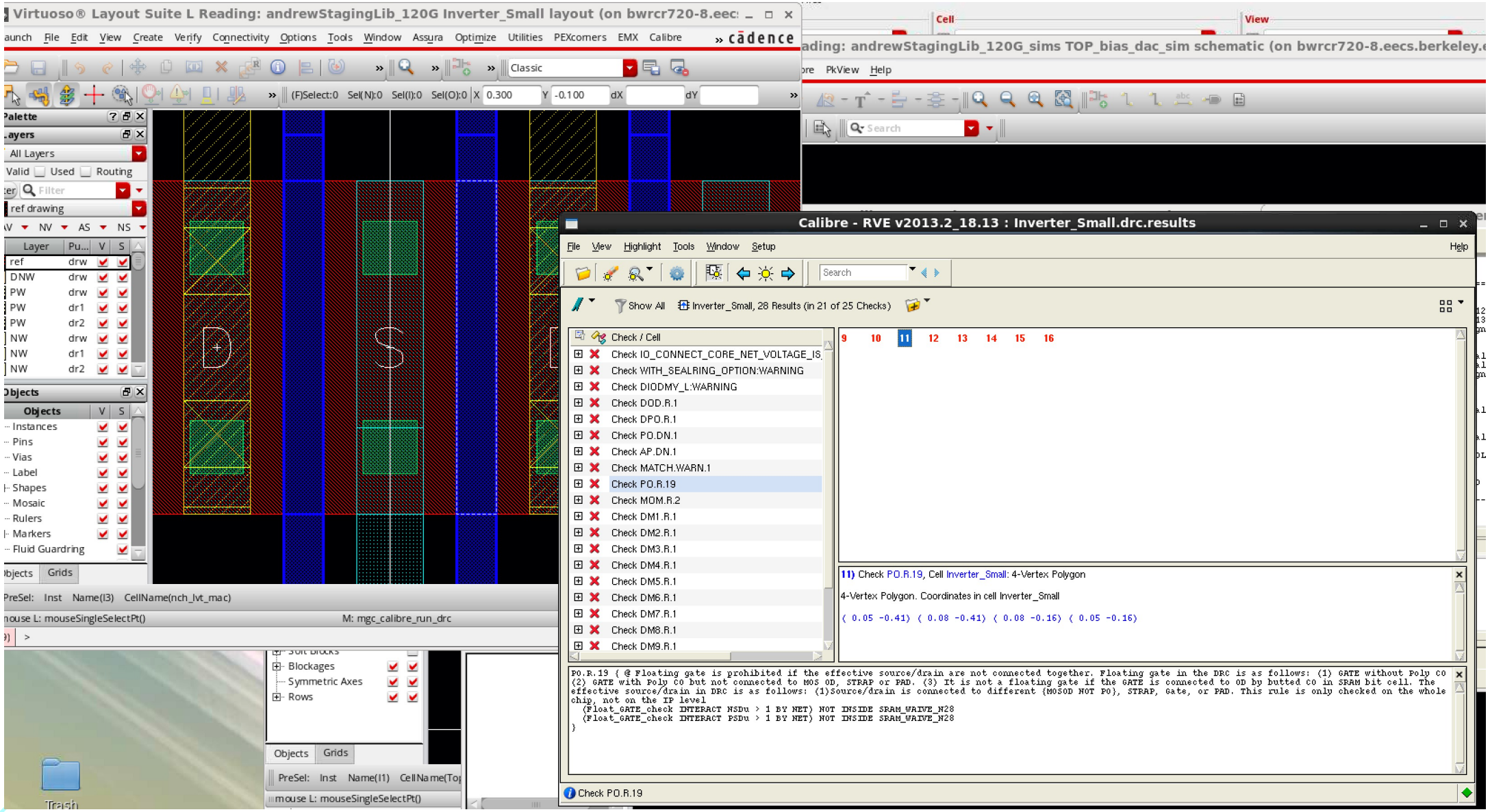
DRC Errors


Calibre - RVE v2013.2_18.13 : Inverter_Small.drc.results
File View Highlight Tools Window Setup Help
Search
Show All
Inverter_Small, 28 Results (in 21 of 25 Checks)
Check / Cell
Check IO_CONNECT_CORE_NET_VOLTAGE_IS
Check WITH_SEALRING_OPTION:WARNING
Check DIODMY_L:WARNING
Check DOD.R.1
Check DPO.R.1
Check PO.DN.1
Check AP.DN.1
Check MATCH.WARN.1
Check PO.R.19
Check MOM.R.2
Check DM1.R.1
Check DM2.R.1
Check DM3.R.1
Check DM4.R.1
Check DM5.R.1
Check DM6.R.1
Check DM7.R.1
Check DM8.R.1
Check DM9.R.1
1
IO_CONNECT_CORE_NET_VOLTAGE_IS_CORE:WARNING1 { @ USE_IO_VOLTAGE_ON_CORE_TO_IO_NET option is off in this DRC run.
@ 1. It will use low voltage space rules to do DRC, as you do not assign the voltage marker & the net connects to IO MOS and core MOS simultaneously
@ 2. If the designer knows some nets use high volatage,
@ please turn on USE_IO_VOLTAGE_ON_CORE_TO_IO_NET option to check high voltage space rules conservatively.
@ 3. If you turn on USE_IO_VOLTAGE_ON_CORE_TO_IO_NET option, you might find some high voltage space violations are actually false errors
@ because these nets actually use low voltage. You can turn off the option.
@ 4. It is strongly recommended to assign volatage marker layer on the nets connect to IO MOS and core MOS simultaneously.
@ 5. This warning is just a reminder, not a gated item for tape-out.
COPY CHIPx
}
Check IO_CONNECT_CORE_NET_VOLTAGE_IS_CORE:WARNING1

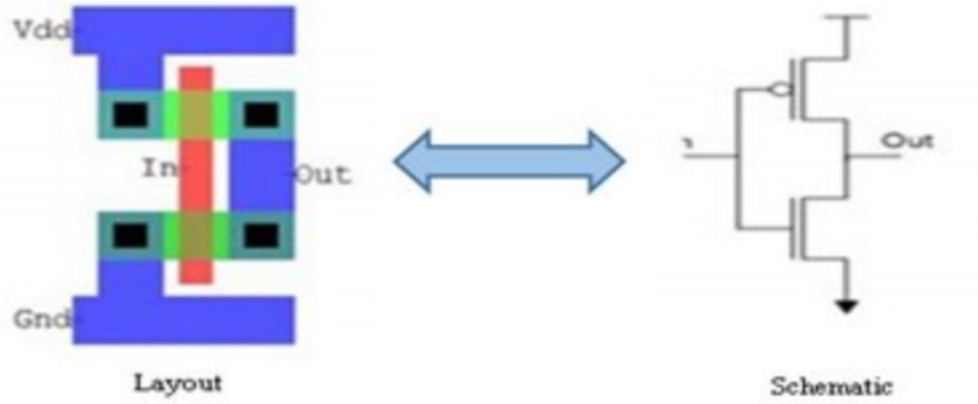
Fixing DRC Errors



Locating the Actual Culprit

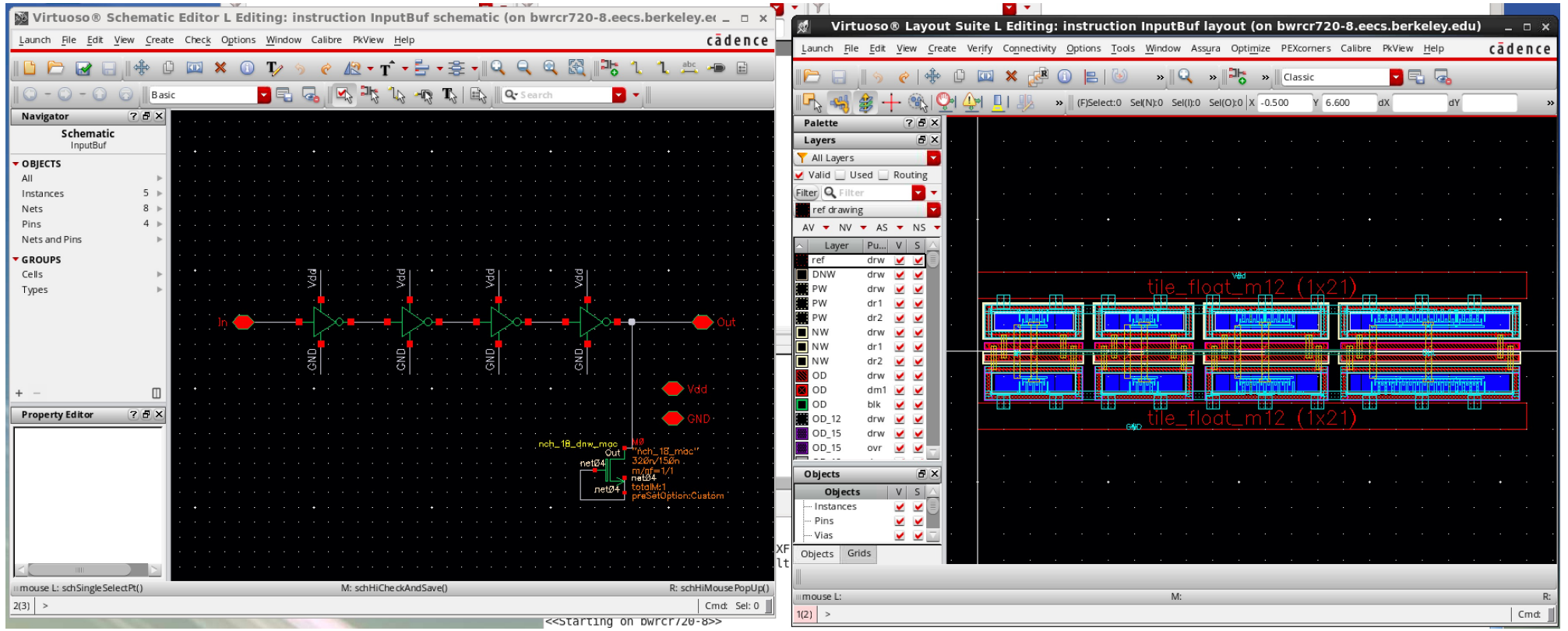


LVS



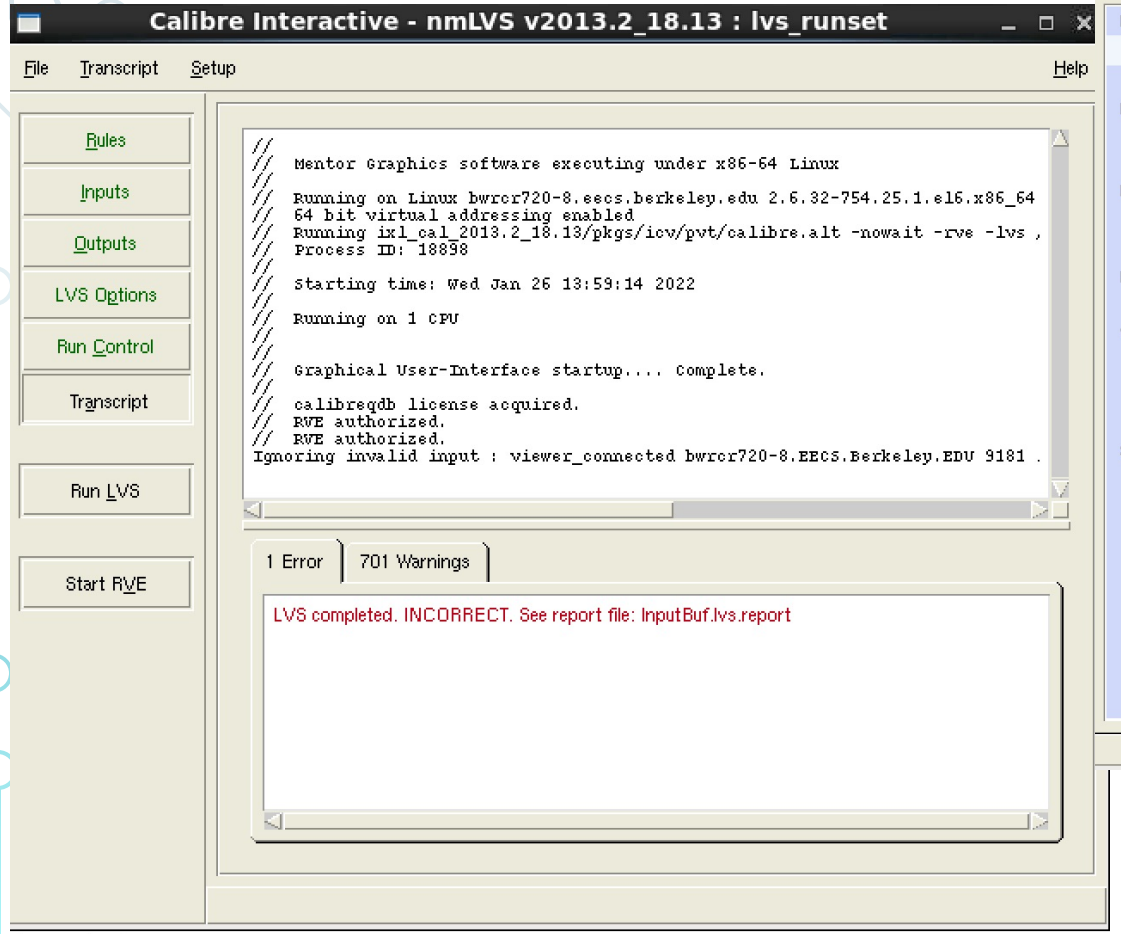
- Layout versus Schematic check to ensure that your layout actually matches your schematic
- This is one of the best (and most painful) things about designing and IC. On one hand, it's very reassuring to know that your layout is correct and you didn't accidentally short VDD to GND. On the other hand, finding and correcting these errors can be extremely challenging in a complex top level layout.

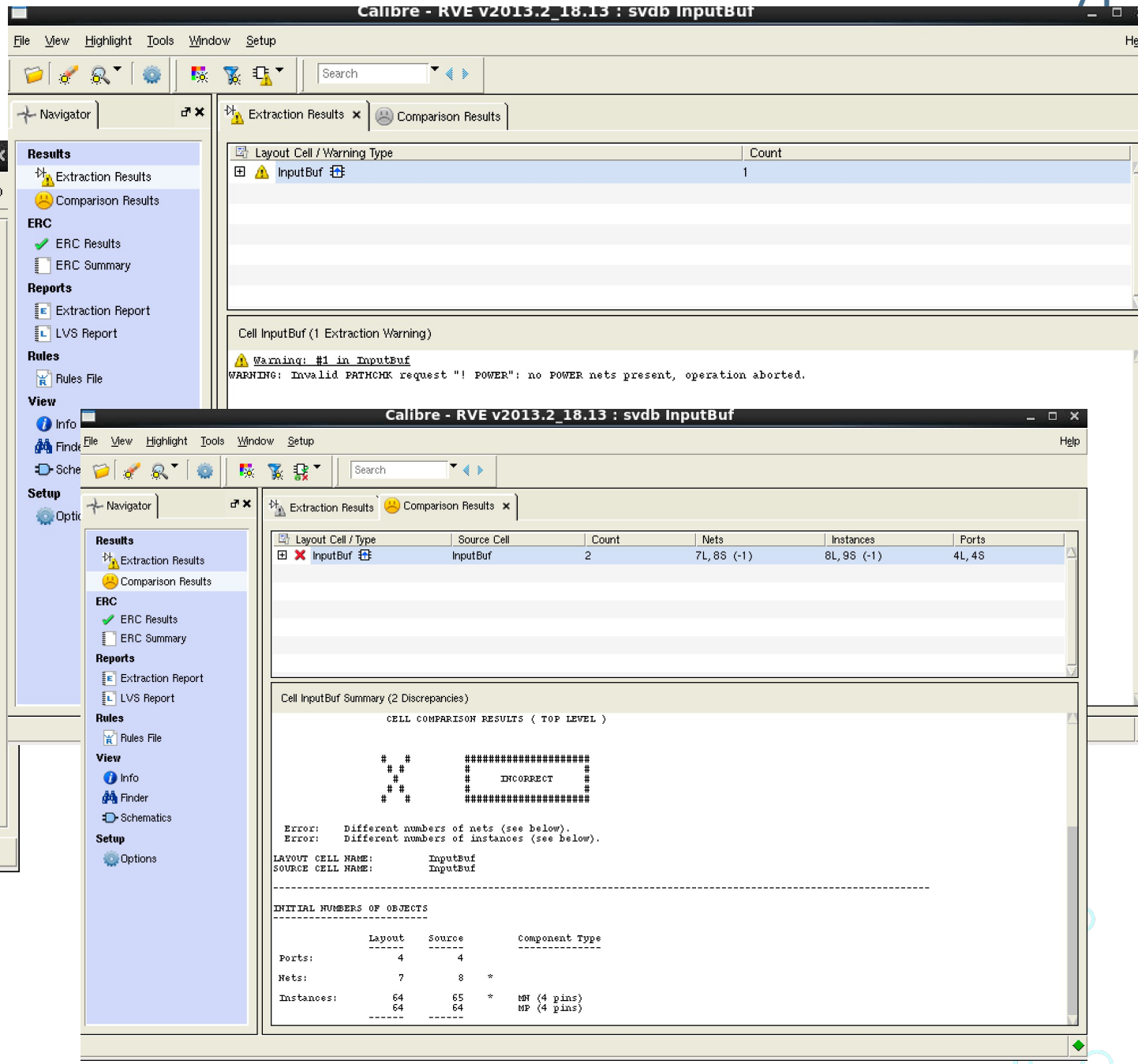
LVS Errors and Fixing



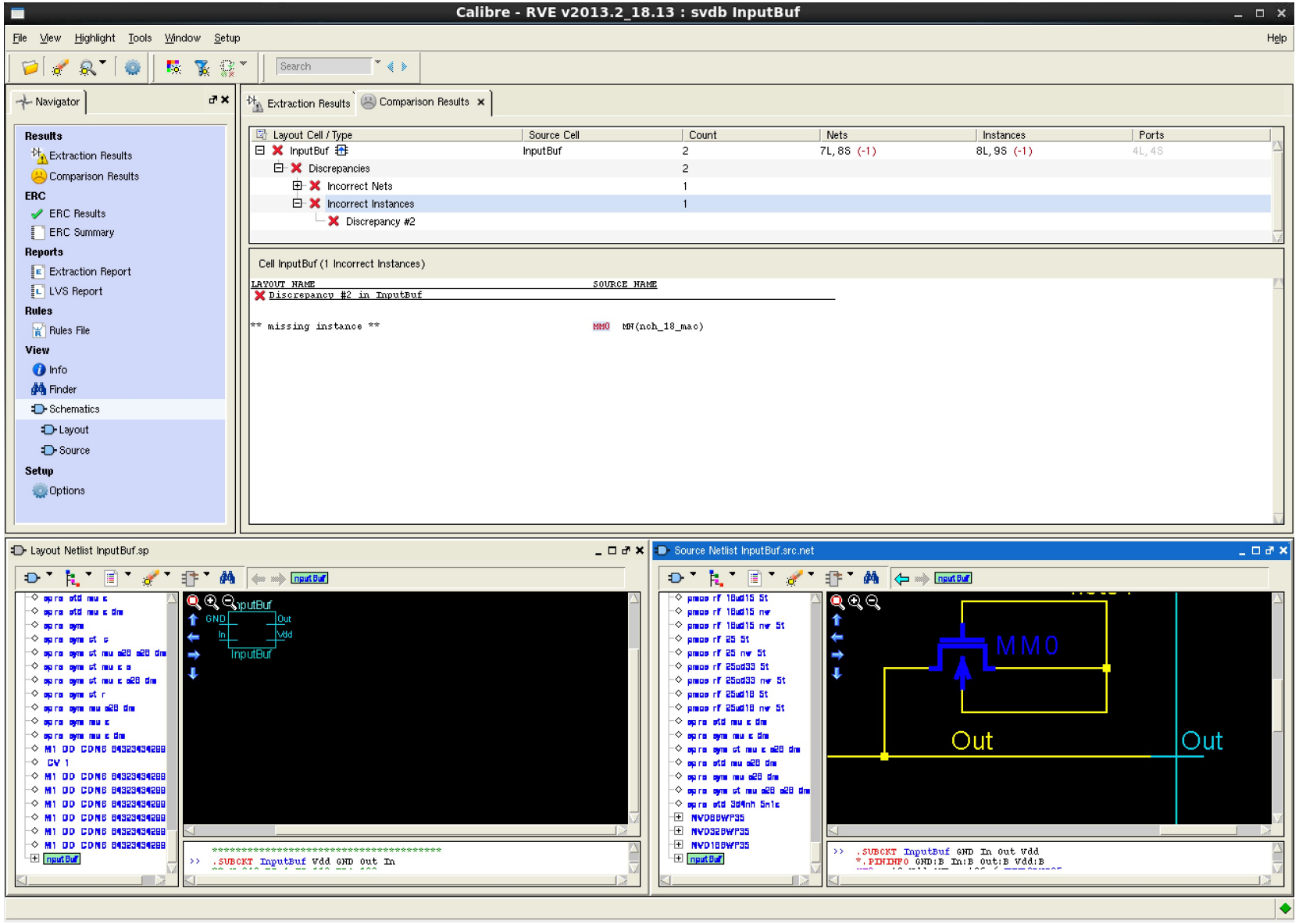
- Example layout and schematic
- Note I've added one extra dummy device to break LVS

LVS Results

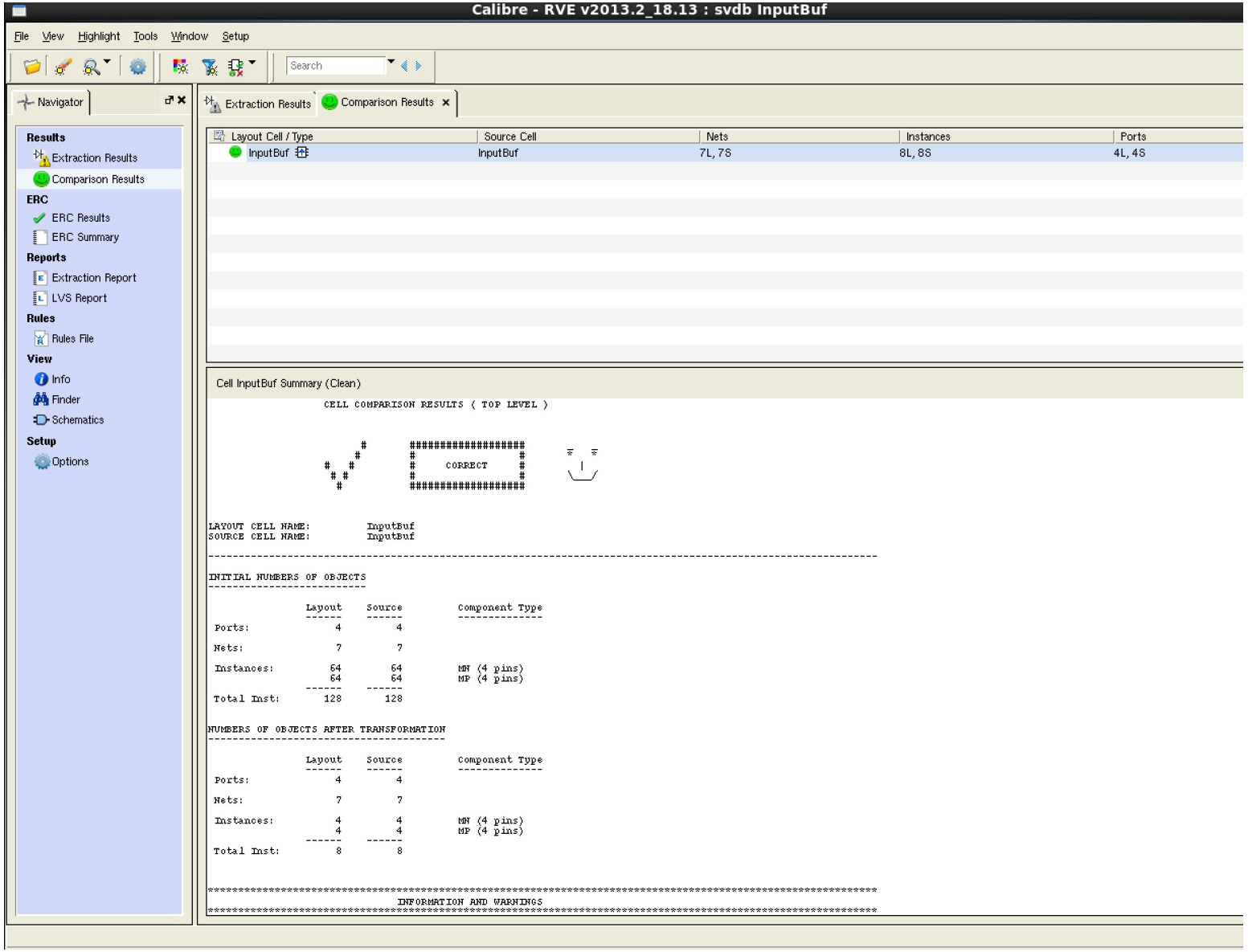

Calibre Interactive - nmLVS v2013.2_18.13 : lvs_runset
File
Transcript
Setup
Help
Rules
Inputs
Outputs
LVS Options
Run Control
Transcript
Run LVS
Start RVE
//
// Mentor Graphics software executing under x86-64 Linux
//
// Running on Linux bwrcr720-8.eecs.berkeley.edu 2.6.32-754.25.1.el6.x86_64
// 64 bit virtual addressing enabled
// Running ixl_cal_2013.2_18.13/pkgs/icv/pvt/calibre.alt -nowait -rve -lvs ,
// Process ID: 18898
//
// Starting time: Wed Jan 26 13:59:14 2022
//
// Running on 1 CPU
//
//
// Graphical User-Interface startup.... Complete.
//
// calibreqdb license acquired.
// RVE authorized.
// RVE authorized.
Ignoring invalid input : viewer_connected bwrcr720-8.EECS.Berkeley.EDU 9181 .
1 Error
701 Warnings
LVS completed. INCORRECT. See report file: InputBuf.lvs.report


Calibre - RVE v2013.2_18.13 : svdb InputBuf
File View Highlight Tools Window Setup
Search
Navigator
Results
Extraction Results
Comparison Results
ERC
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Extraction Results
Comparison Results
Layout Cell / Warning Type
Count
InputBuf
1
Cell InputBuf (1 Extraction Warning)
Warning: #1 in InputBuf
WARNING: Invalid PATHCHK request "! POWER": no POWER nets present, operation aborted.
Calibre - RVE v2013.2_18.13 : svdb InputBuf
Layout Cell / Type
Source Cell
Count
Nets
Instances
Ports
InputBuf
InputBuf
2
7L, 8S (-1)
8L, 9S (-1)
4L, 4S
Cell InputBuf Summary (2 Discrepancies)
CELL COMPARISON RESULTS (TOP LEVEL)
INCORRECT
Error: Different numbers of nets (see below).
Error: Different numbers of instances (see below).
LAYOUT CELL NAME: InputBuf
SOURCE CELL NAME: InputBuf
INITIAL NUMBERS OF OBJECTS
Layout
Source
Component Type
Ports: 4 4
Nets: 7 8 *
Instances: 64 65 * MN (4 pins)
64 64 MP (4 pins)

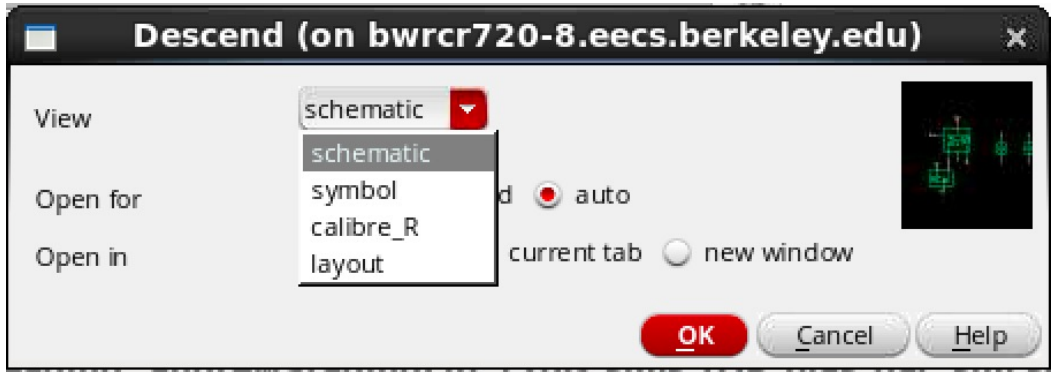
Details


Calibre - RVE v2013.2_18.13 : svdb InputBuf
File View Highlight Tools Window Setup Help
Navigator
Results
Extraction Results
Comparison Results
ERC
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Layout
Source
Setup
Options
Extraction Results
Comparison Results
Layout Cell / Type
Source Cell
Count
Nets
Instances
Ports
InputBuf
Discrepancies
Incorrect Nets
Incorrect Instances
Discrepancy #2
Cell InputBuf (1 Incorrect Instances)
LAYOUT NAME
SOURCE NAME
Discrepancy #2 in InputBuf
** missing instance **
MM0 MN(nch_18_mac)
Layout Netlist InputBuf.sp
Source Netlist InputBuf.src.net
GND
In
Out
Vdd
InputBuf
MM0
Out
Out

The Best Smile You'll Ever See

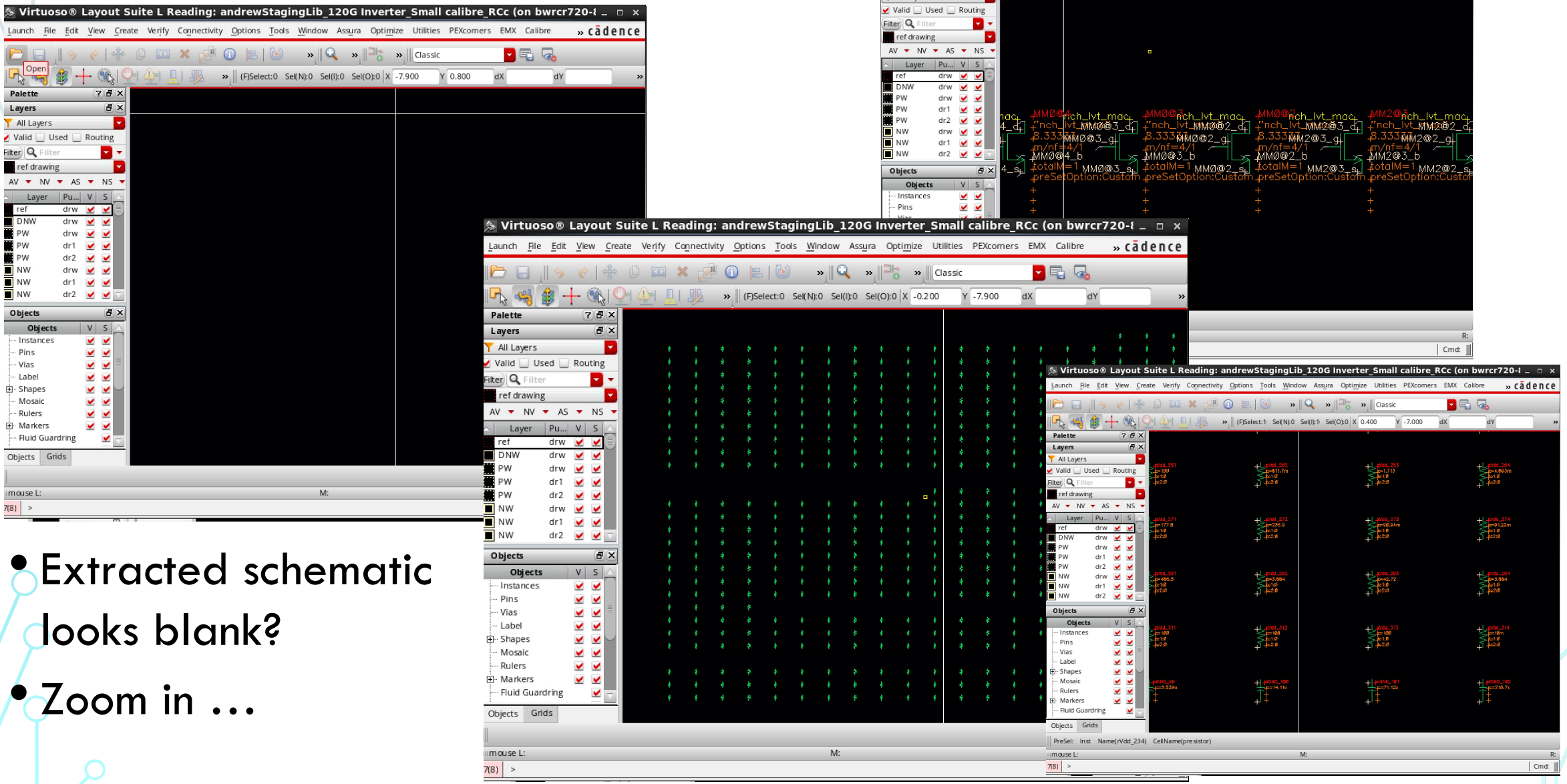


Extraction



- Layout adds parasitics not in your schematic
- Capacitance of wires and poly
- Extra routing resistance
- Extraction is used to estimate these parasitics:
  - C only, groudned
  - C coupled
  - RC
  - R only (useful for low frequency IR drop analysis)
- Another benefit of extraction is layout dependent shifts are also added to instances of transistors (well proximity effect)
- After running extraction, you create a “calibre” view (you can name it anything)

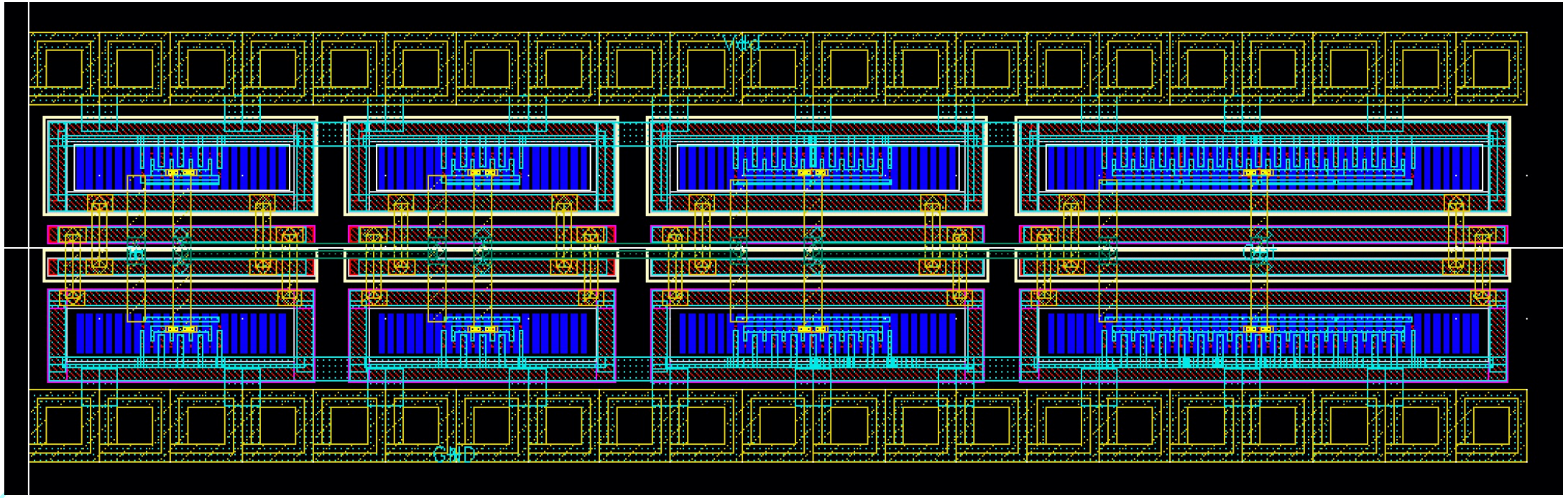
Extracted Netlists



- Extracted schematic looks blank?
- Zoom in …

Top Level Example

- Top level should have pins that are on periphery to make routing easy
- VDD and VSS should be clearly visible and robust
- Follow conventions on routing
  - Horizontal / vertical can be on even/odd layers
- Avoid using top metals in cells and use these metals for global routing



ERC

- Electrical rules
- Current density limits especially in aluminum
  - Depends on temperature and duty cycle, different for AC vs DC
- Poly has very limited current handling capability
- Antenna errors
  - Antenna diodes
- LUP errors

References

- Lienig, Scheible, "Fundamentals of Layout Design for Electronic Circuits," Springer 2020.
- Maloberti, F, "Layout of Analog CMOS Integrated Circuits" (Part 2)
- Hastings, "The art of analog layout," Prentice Hall, 2001.