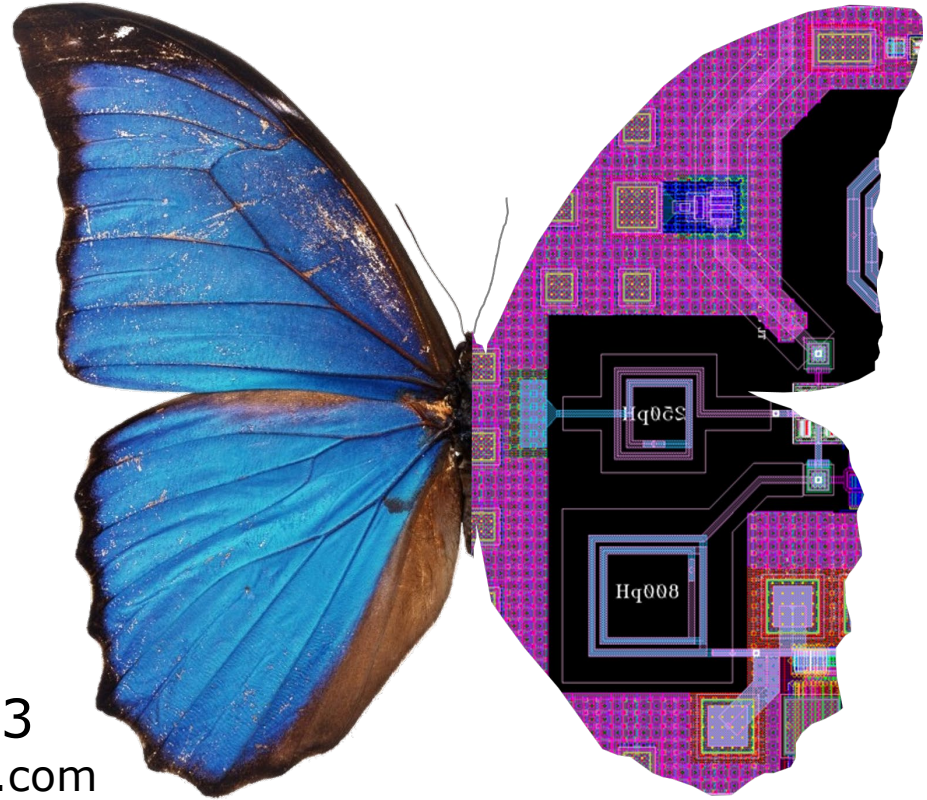
The Art of mm-Wave Design & Layout



Shahriar Shahramian
Nokia – Bell Laboratories – 2023
Shahriar.Shahramian@Nokia-Bell-Labs.com

Tutorial Outline

- Introduction
- Mm-Wave layout philosophy & approach
- Design examples & common layout mistakes
- Passive & active structures
- Challenges of complex mm-wave ASICs
- Packaging and the near-THz era

Introduction

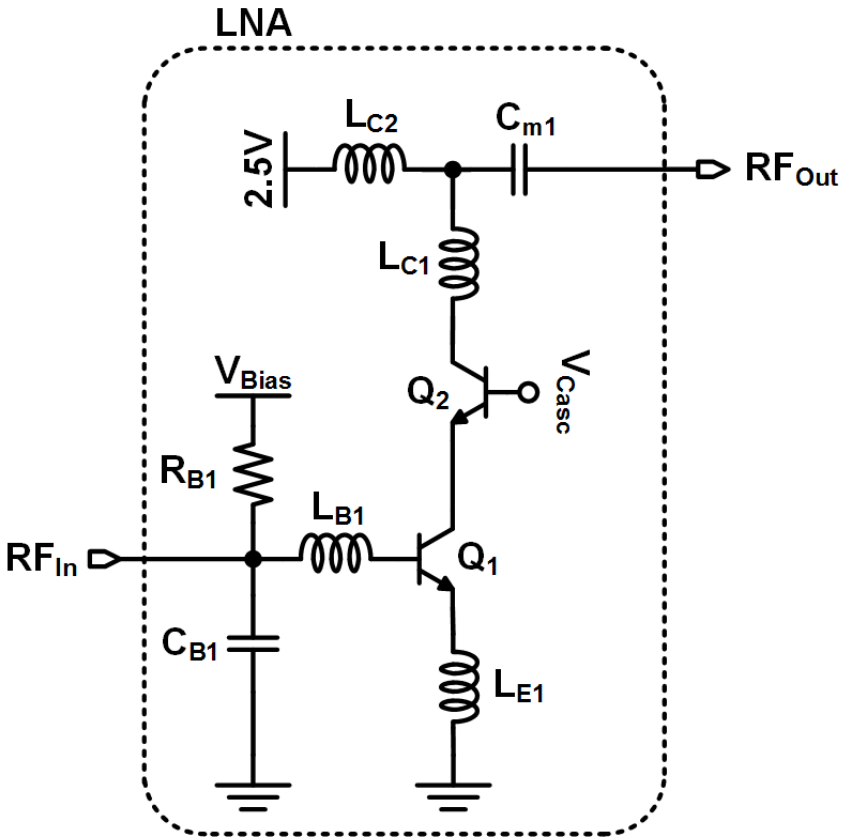
- Mm-Wave systems require a combination of circuit and layout innovations
  - Mm-Wave layout demands mm-wave design expertise
- Mm-Wave design and layout is an inherently iterative process
  - Software developers continue to streamline this process (or try to…)
- Developing a systematic methodology is critical especially for large systems
  - Schematic, extraction, EM simulation, modelling, etc.
- There are no shortcuts, every micron matters!
- Higher frequency circuits are less forgiving to poor layout
  - Power distribution, decoupling requirements do not scale with frequency
- Do not forget analog layout techniques, they still matter!

Design Example: W-Band LNA

- Looks simple enough!

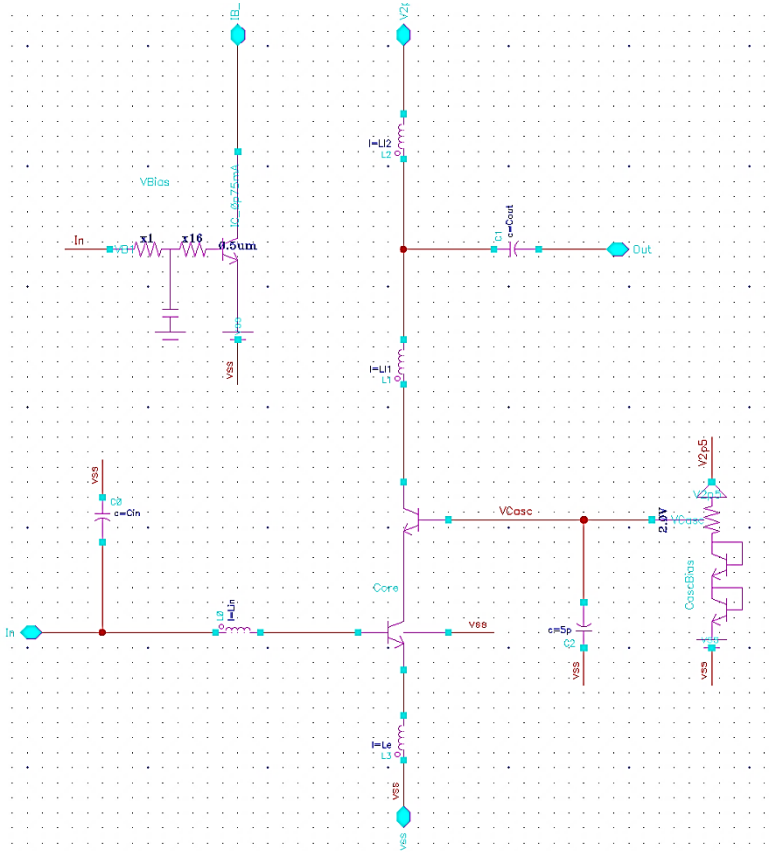
- Center frequency: 90GHz
- Optimize for NF & Gain
- Input return loss <-15dB (S11)
- Digital DC bias control (V_{Bias})
- Self-bias of Cascode node (V_{Casc})
- Minimize layout footprint

- Minimize power consumption
- Aim for bandwidth >10GHz

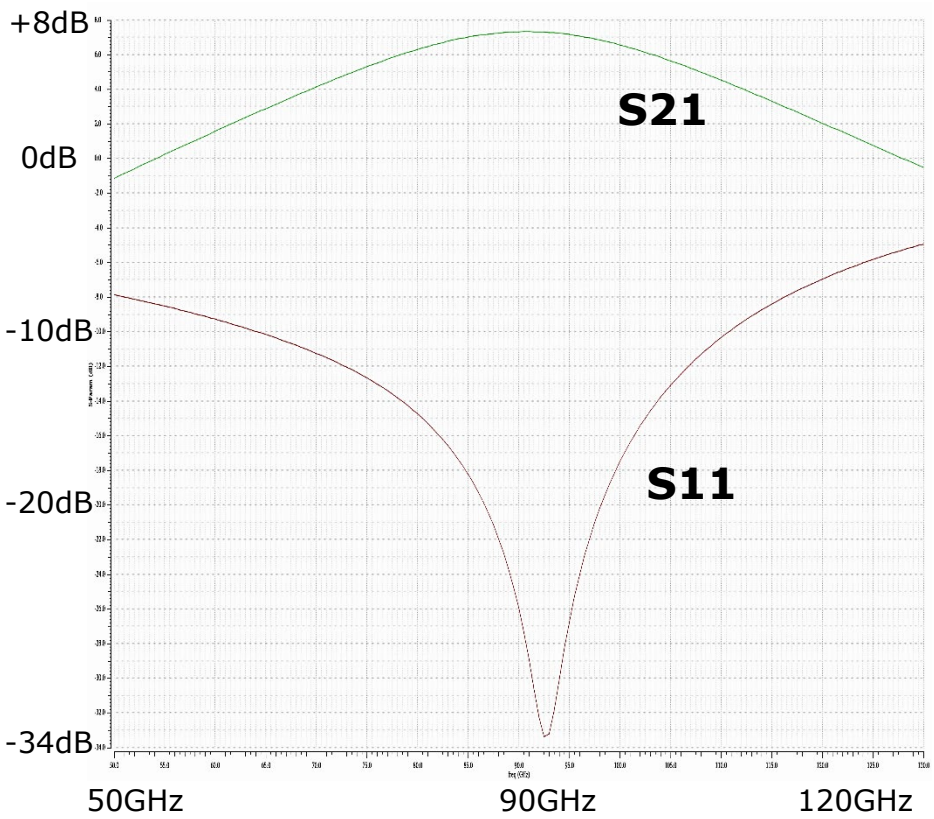


Design Example: W-Band LNA

- Transfer schematic into CAD tool
- Using design-kit device models
  - HBTs – What parasitics do they include?
- Ideal passives as initial pass
  - Capacitors, resistors, inductors, etc.
- Optimize circuit parameters:
  - Transistor size, bias current density
  - Optimum source impedance
  - Matching network topologies
  - Biasing networks & passive values
  - Typical operation temperature & V_{DD}
  - *Ensure correct DC operating point!*



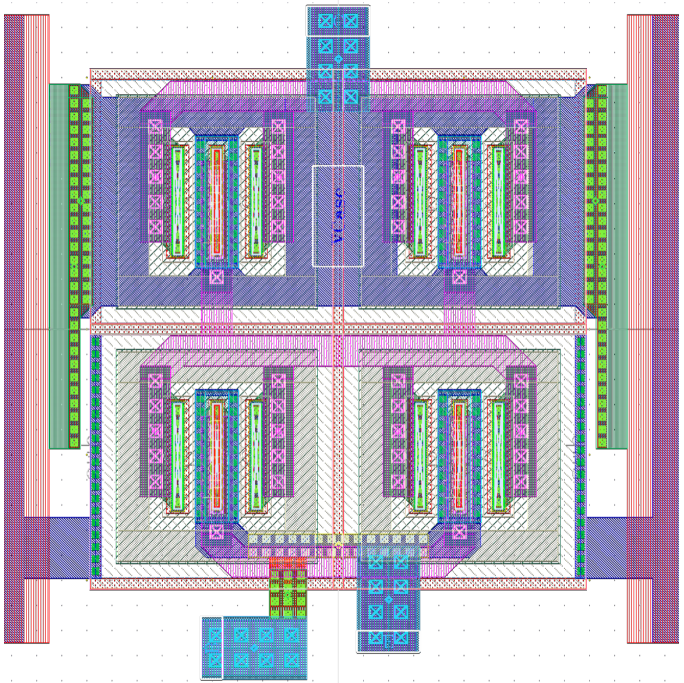
Foundry HBT Models & Ideal Passives

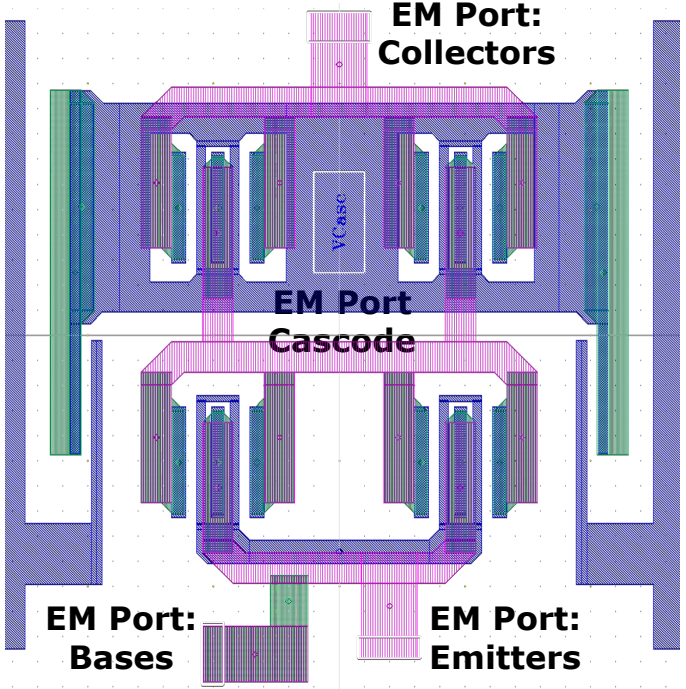


- First pass S-parameters simulations look very good! But we have a long way to go…
- At 90GHz, the circuit is very sensitive to even small amounts of parasitics.
- Which part of the circuit should we extract first?

LNA Core Devices (HBT) EM Layout

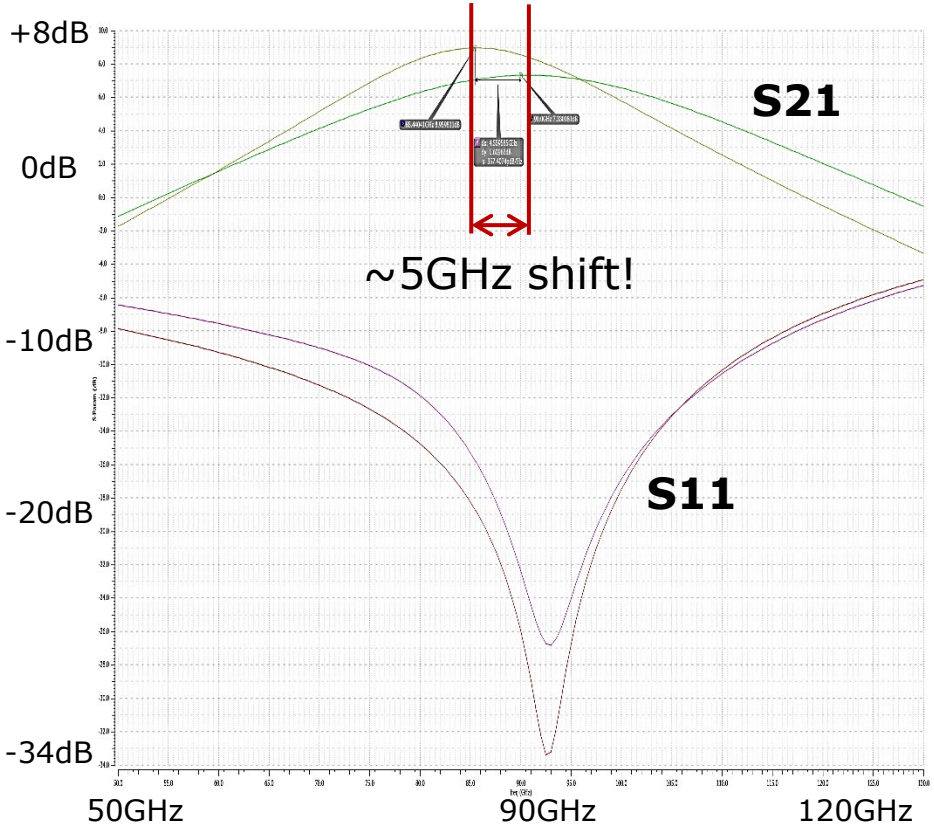
C M1 M2 M3 M4 M5 M6 M7





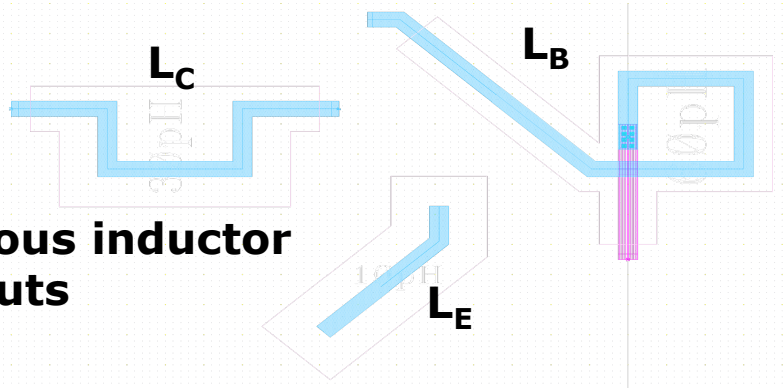
- Core HBT layout includes foundry HBT P-Cells as well as metallization to reach higher metal layers
- Removing the HBTs leaves only the metallization which are *not* included in the foundry device models. This is a crucial step!

HBT Models, Core EM Extraction & Ideal Passives



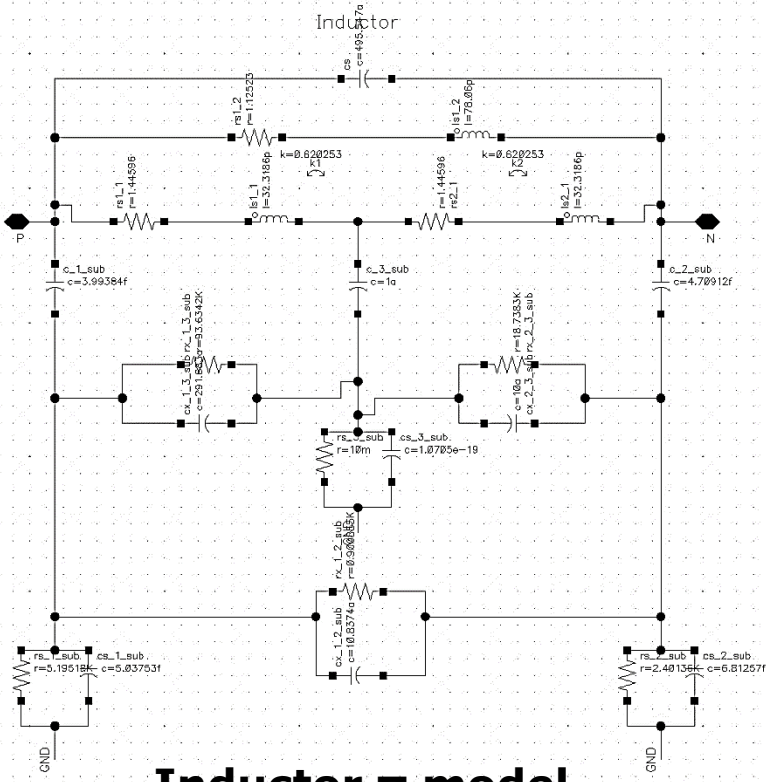
- The ~5GHz shift in the center frequency is *only* due to the very small parasitics of the core HBT layout
- With the new LNA core EM model, we can re-optimize circuit passive components values

Inductor Design & Modelling



Various inductor layouts

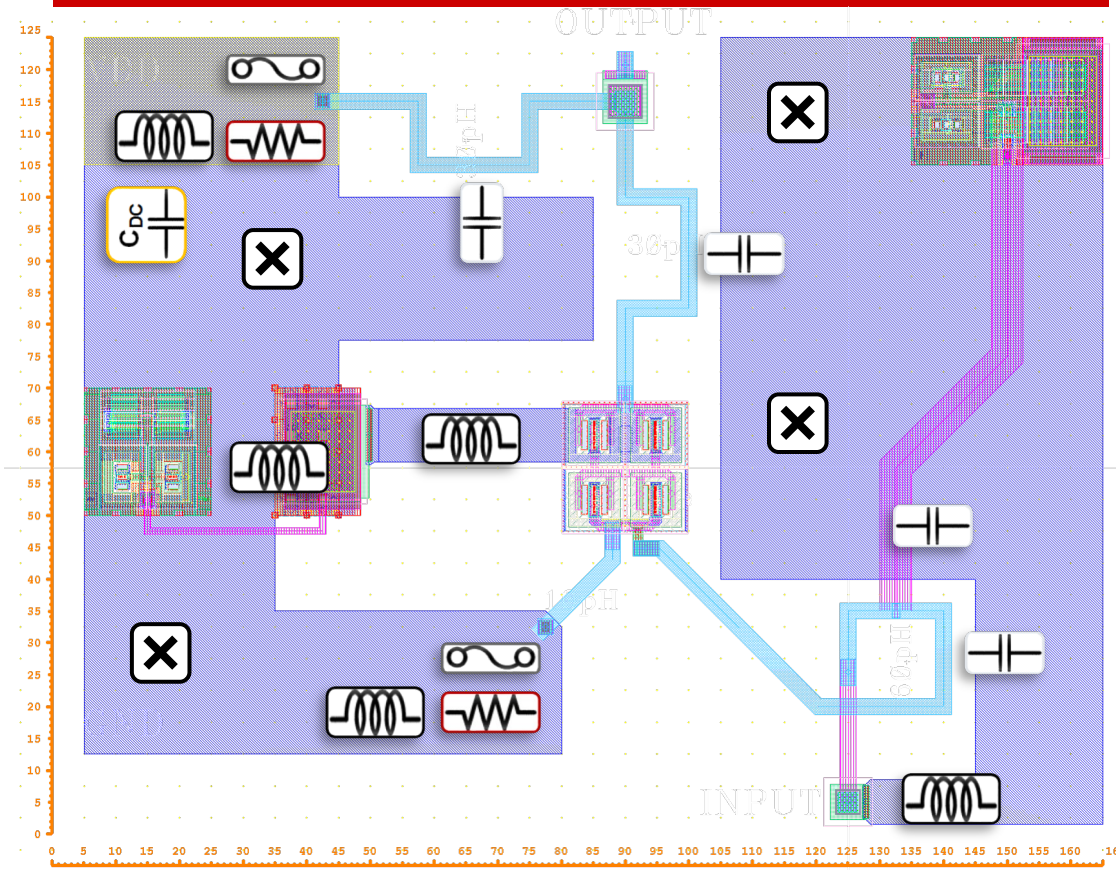
- A π inductor model can be used in place of an ideal inductor. This model can be manually tweaked to converge to the desired parameters
- This model captures inductor Q, self-resonance frequency, substrate interactions, substrate losses, etc.
- Be ready to perform many EM iterations!



Inductor π model

W-Band LNA (Poor!) Layout

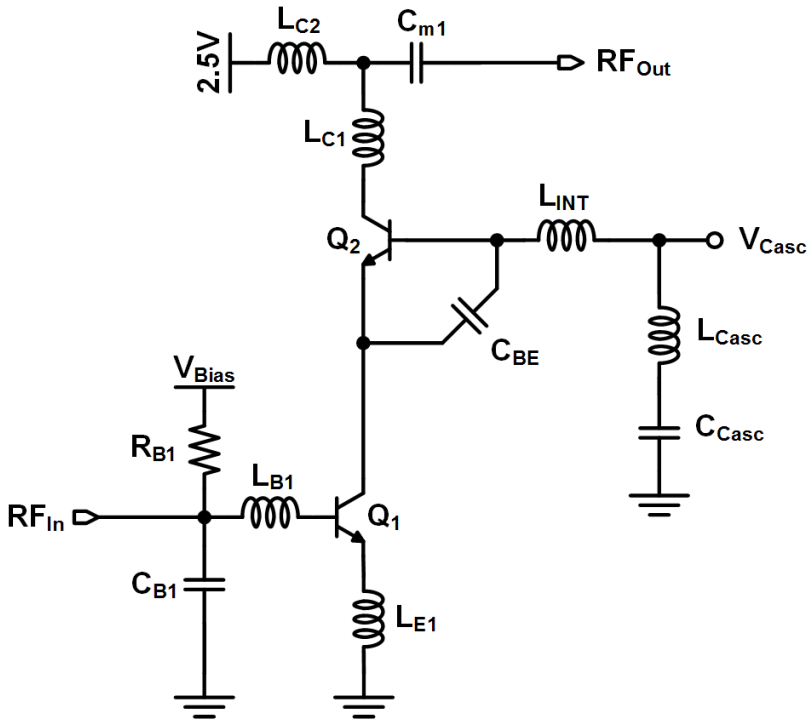
C M1 M2 M3 M4 M5 M6 M7



- This layout passes all LVS & DRC rules and can be manufactured. However, it suffers fundamental flaws!
- Undesired inductance:
- Undesired capacitance:
- Undesired resistance:
- No VDD decoupling:
- No substrate contacts:
- Failing electromigration:

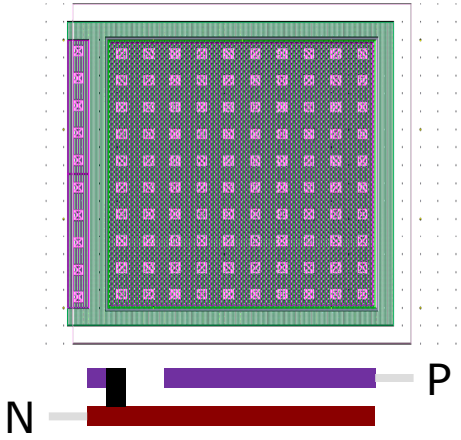
Cascode Node Biasing Considerations

- How should we treat the Cascode node from DC & RF point of view?
- A Highly sensitive node to parasitic inductances. Note the resemblance to a Colpitts oscillator!
- Focus on interconnects, capacitor type, parasitic inductance and impedance of the node as a function of frequency

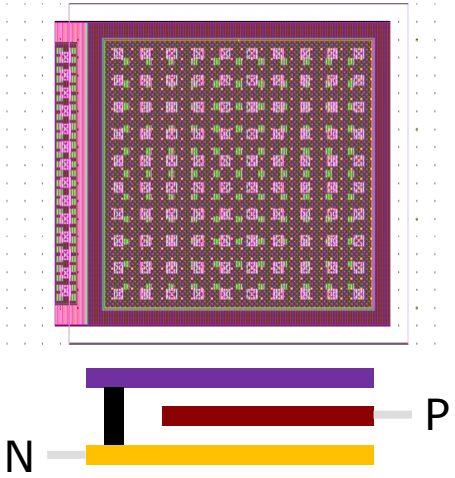


Capacitor Considerations at RF & DC

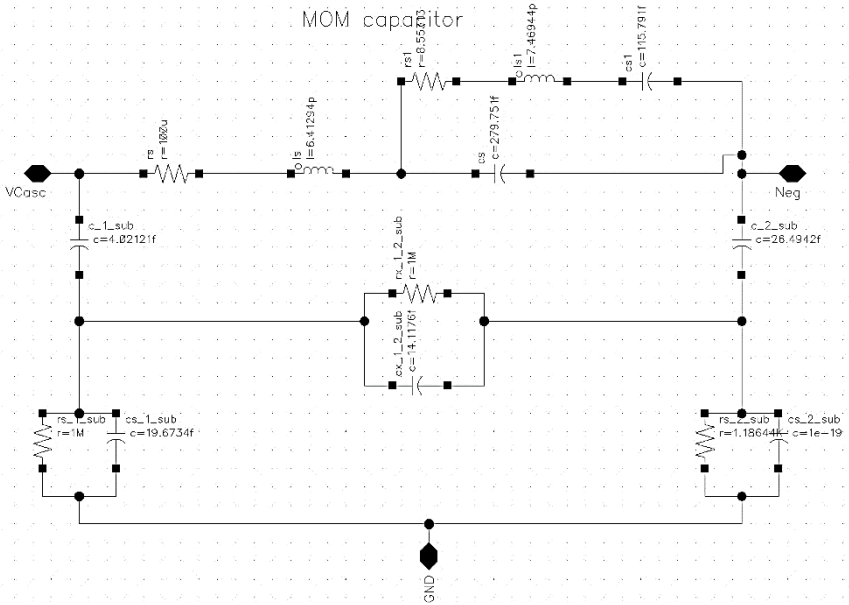
C M1 M2 M3 M4 M5 M6 M7



Single-layer
C_{DC} = 600fF



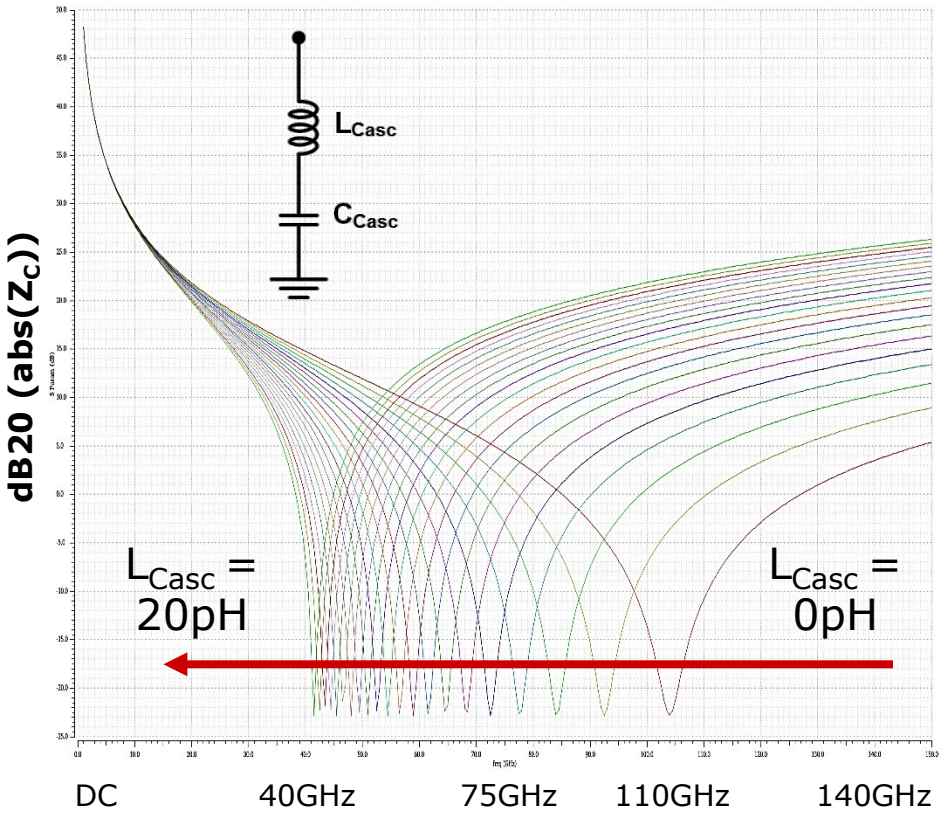
Dual-layer
C_{DC} = 1.2pF



- Single & dual-layer capacitors have different parasitic characteristics & therefore have pros & cons depending on use-case

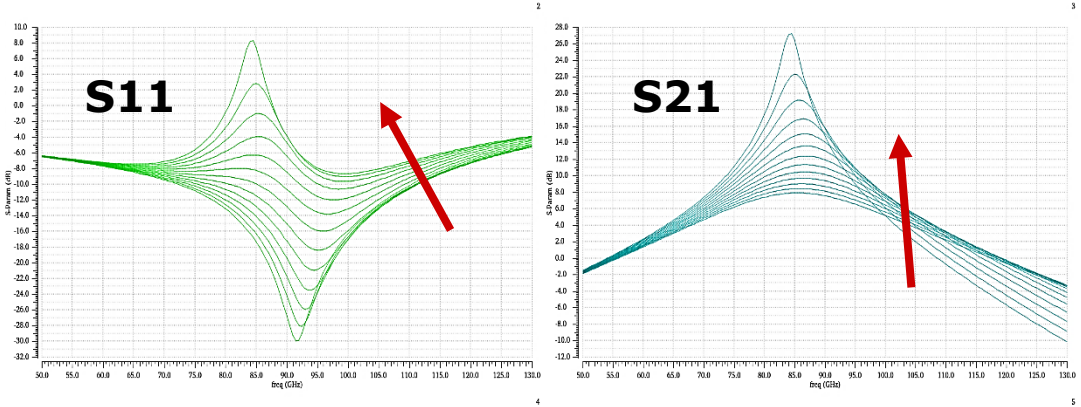
- A capacitor π model captures self-resonance frequency as well as substrate parasitic loading from bottom plate.

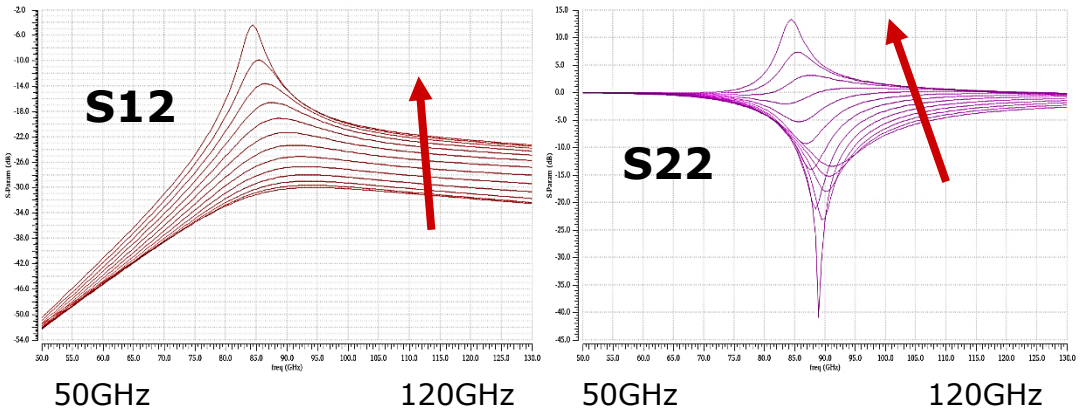
Interconnect Impact on Capacitor Performance



- A relatively small parasitic inductance (20pH) reduces the self-resonance frequency of the Cascode capacitor from 110GHz to nearly 40GHz!
- At resonance, the Cascode node decoupling capacitor is entirely ineffective
- What is the consequence of this on the LNA S-parameters?

Impact of Cascode Inductance on LNA S-Parameters

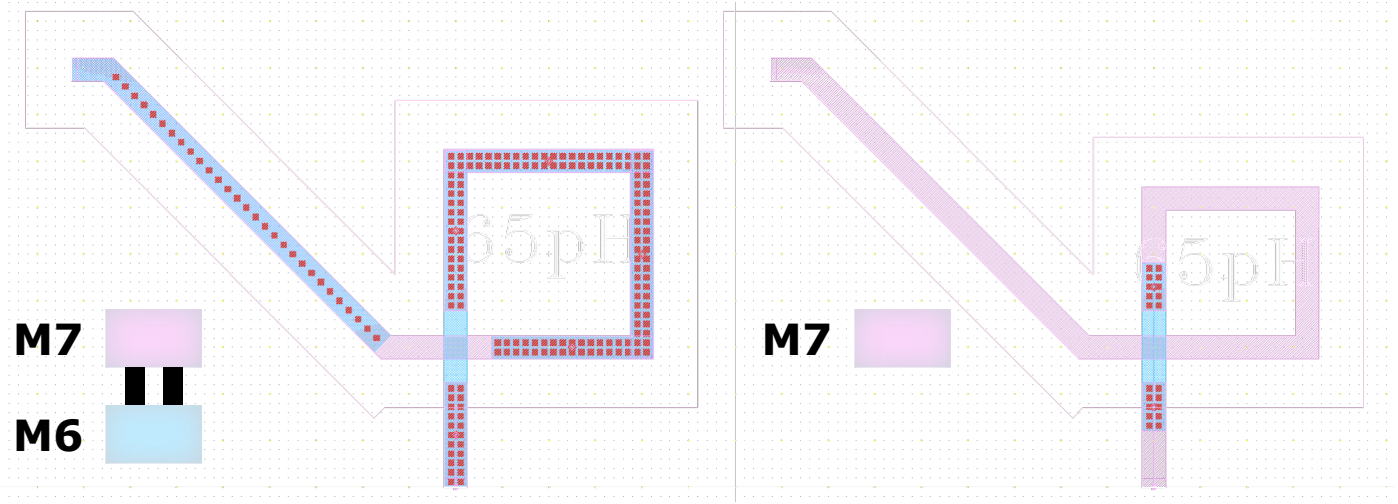




50GHz 120GHz 50GHz 120GHz

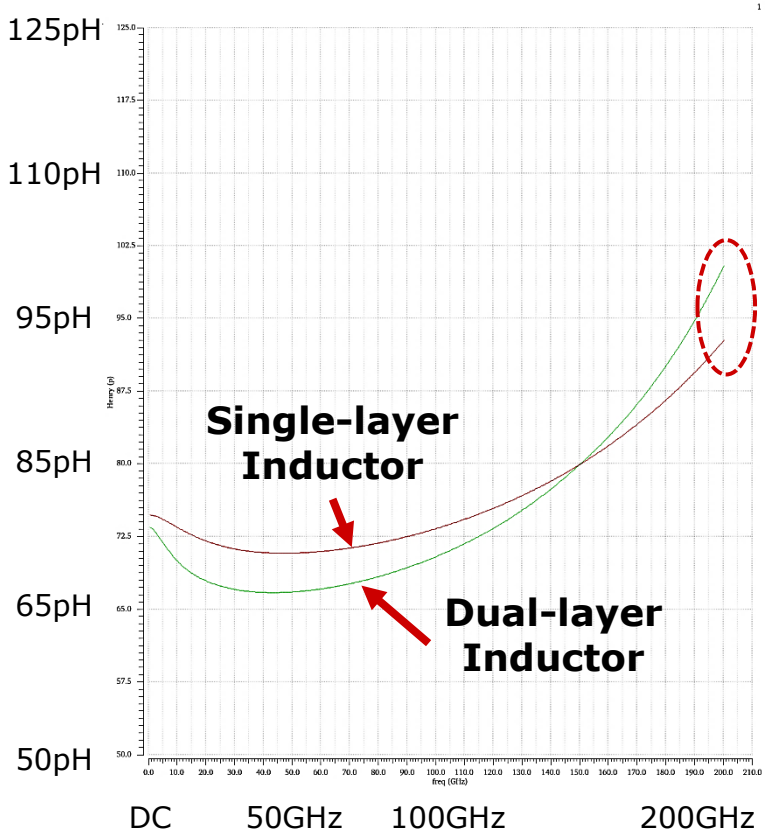
- Predictably, the LNA s-parameters points to circuit instability as the parasitic inductance (L_{Casc}) is swept from 0pH to 20pH
- Note that 20pH of parasitic inductance can arise from a 20um interconnect!
- Careful layout & EM modelling of the Cascode node is needed at mm-Wave frequency ranges

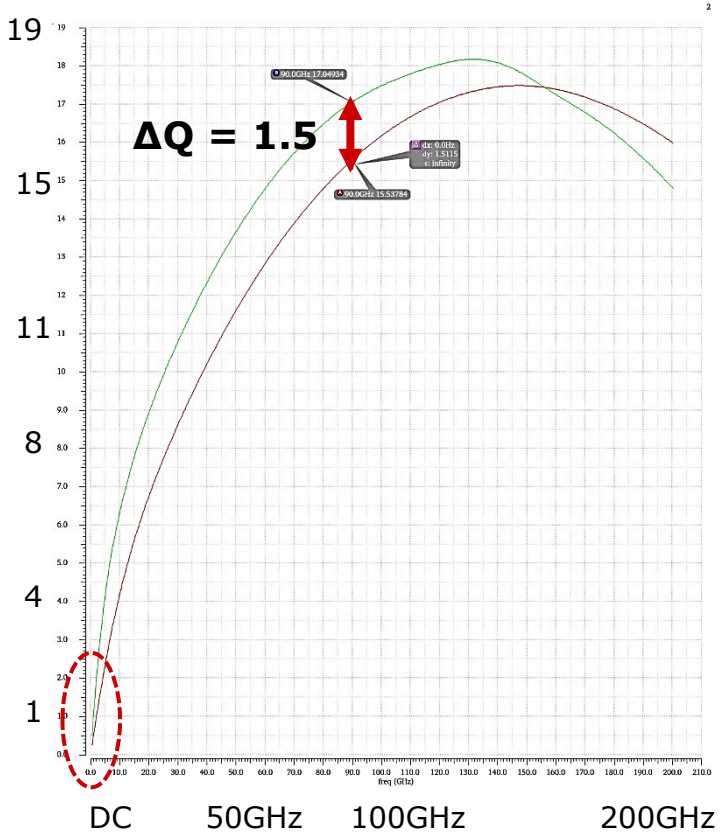
Multi-Layer Inductors at mm-Wave Frequencies



- Single-layer versus multi-layer inductor realization can be used to tradeoff various inductor performance parameters such as quality factor (Q), self-resonance frequency, DC resistance as well as electromigration ratings
- Note that lowering the DC resistance (or Q) isn't always necessary or even preferred!

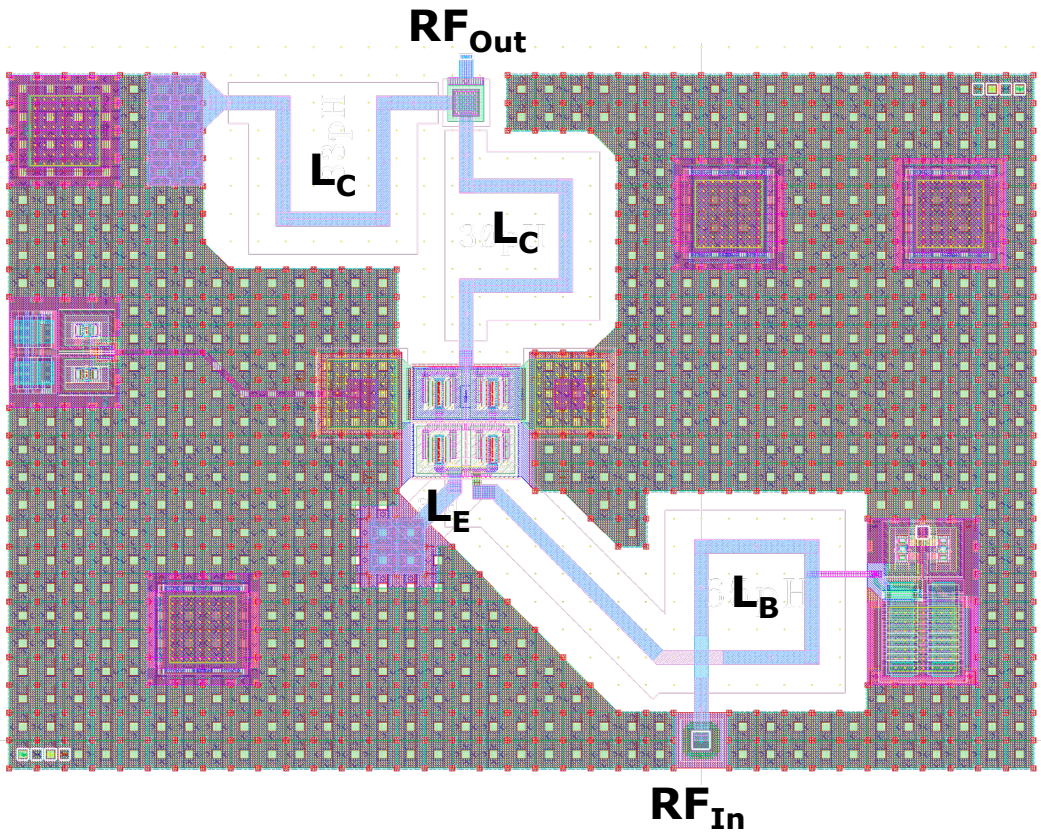
Multi-Layer vs Single-Layer Inductor Performance





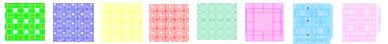
W-Band LNA Improved Layout

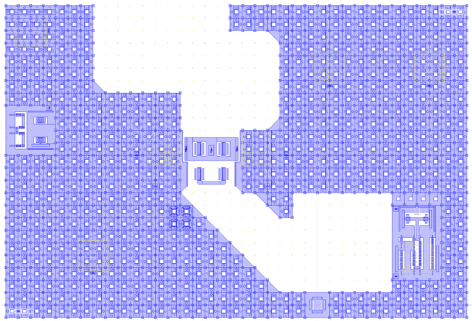
C M1 M2 M3 M4 M5 M6 M7



- Note the significant improvements to the final LNA layout:
  - Quasi-solid GND & V_{DD} planes
  - Minimized Cascode parasitic inductances & optimum decoupling capacitor selection
  - Minimized parasitics on input biasing while maintaining good current mirror matching using analog techniques
  - GND & V_{DD} decoupling capacitors uniformly placed in the supply planes

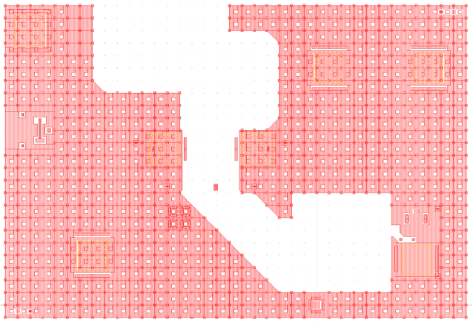
W-Band LNA Layout Layer Utilization



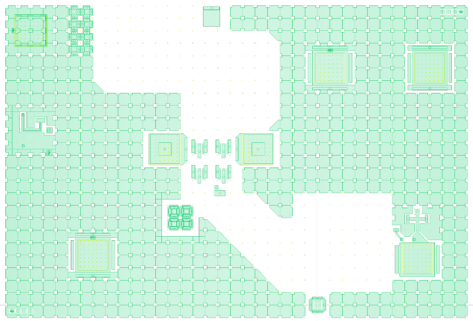


Metal 1

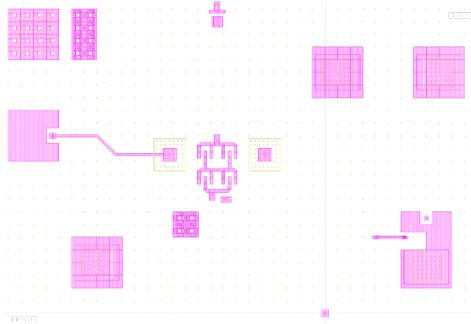
Metal 2



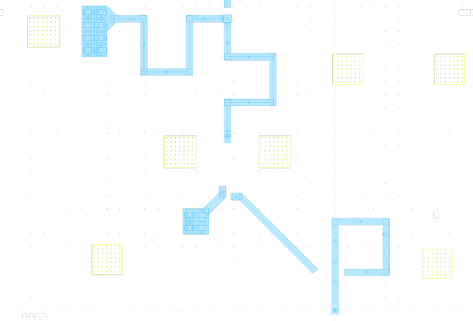
Metal 3



Metal 4

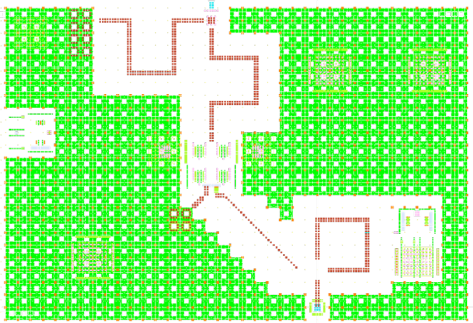


Metal 5



Metal 6

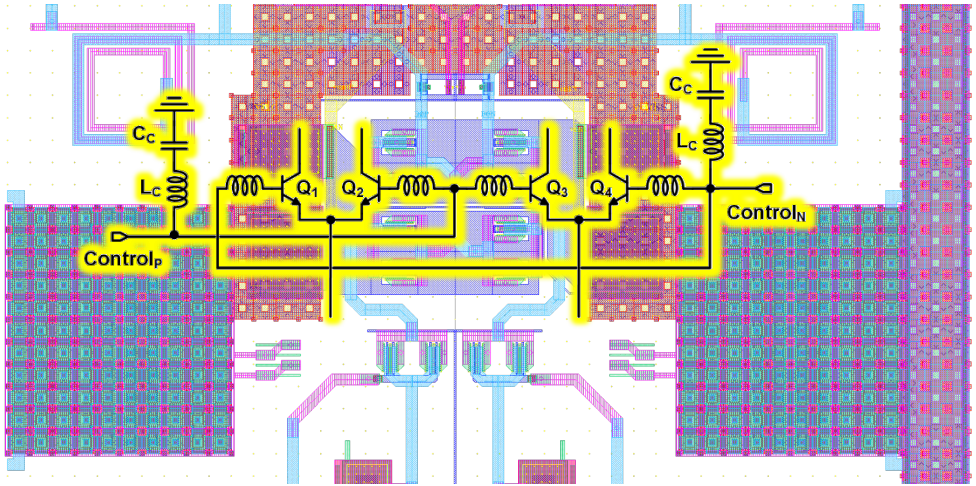
Metal 7

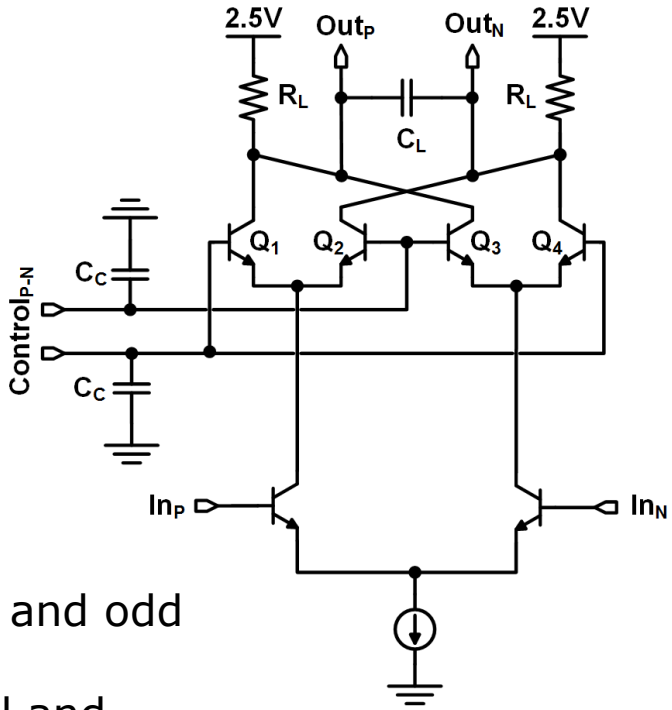


Contacts & VIAs

- Highest allowable density on GND & V_{DD} planes as well as high-capacitance bias layers
- Should we perform a complete EM simulation of the entire block?

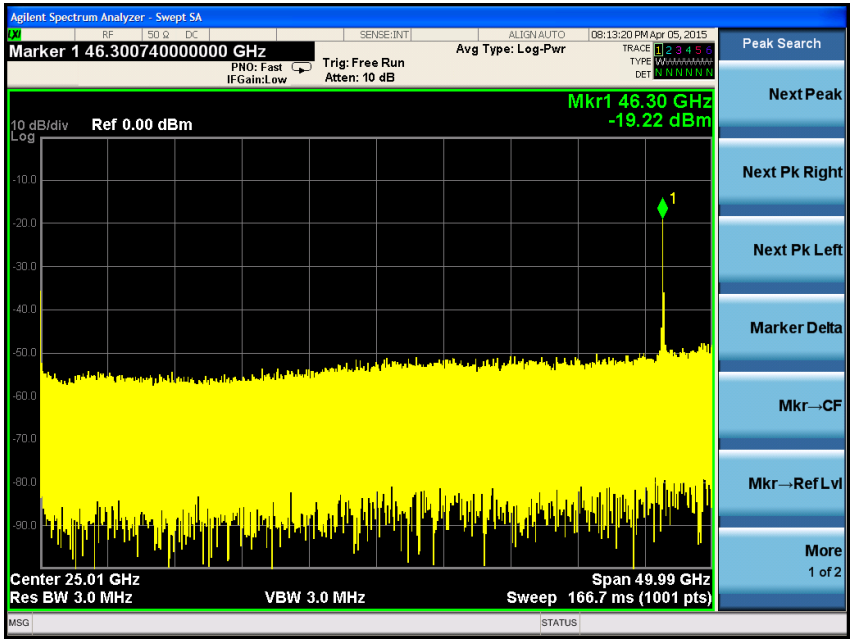
56G/s Output Driver/VGA Problem





- Differential topology offers clear advantages
- Must consider the Cascode VGA node in both even and odd excitation modes
- Different set of parasitics are present in differential and common-mode
- Oscillations can arise in common-mode only!

Output Driver/VGA Common-mode Oscillation

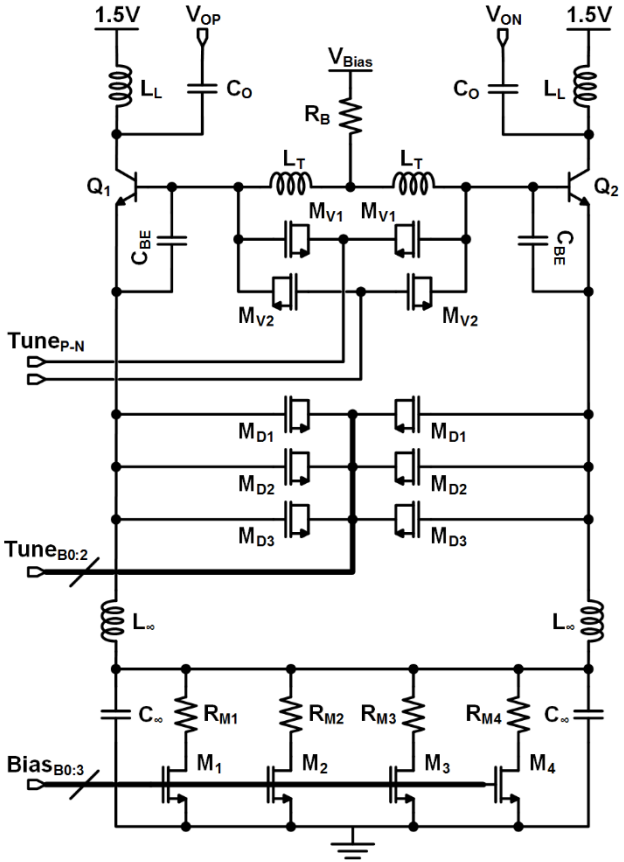


- Common-mode oscillation measured at ~46GHz from the driver IC. No input signal is applied to the device.

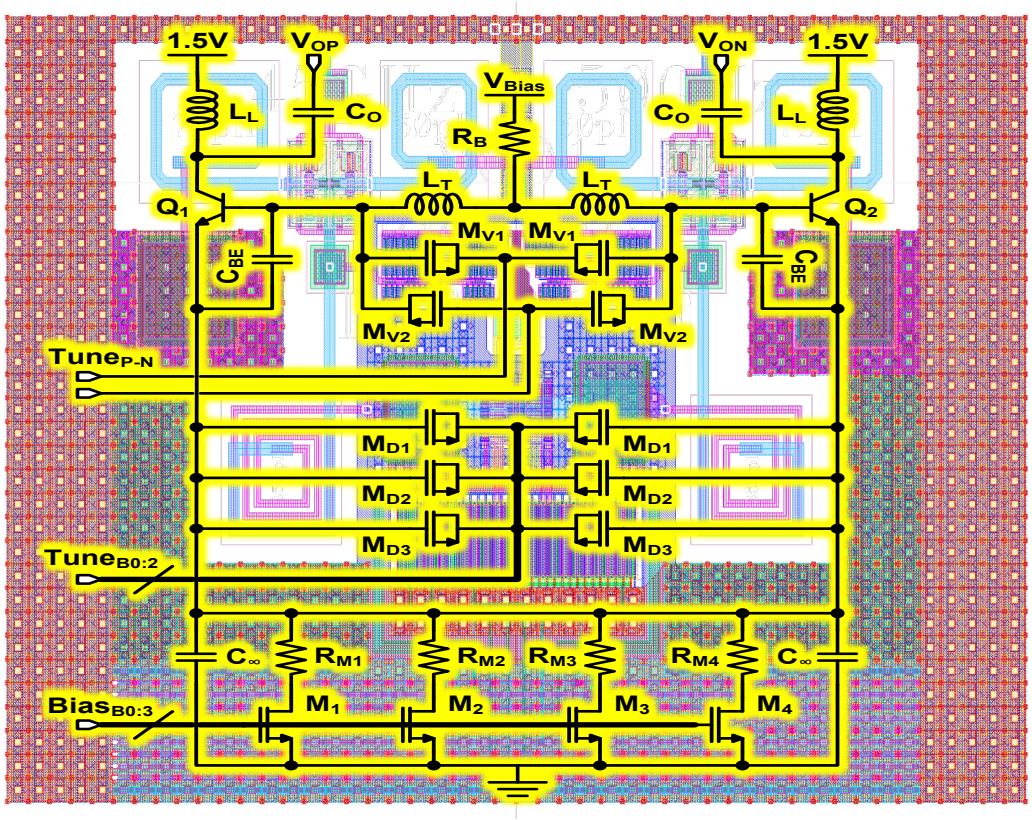
- Oscillation mode can be detected by first measuring the circuit single-ended followed by a measurement using an external balun.
- The interface between the driver and balun must be kept matched in phase & amplitude.

Design Example: 45GHz Colpitts VCO

- Desired center frequency f = 45GHz
  - Optimize for highest overall tunning range
- Optimize for phase noise and output signal swing
  - Strong function of VCO tank quality factor
- Single 1.5V power supply operation
  - Possible since a single HBT is used
- Digital course frequency selection and differential analog tuning
  - Leverage the benefits of SiGe BiCMOS technology (HBT + CMOS)



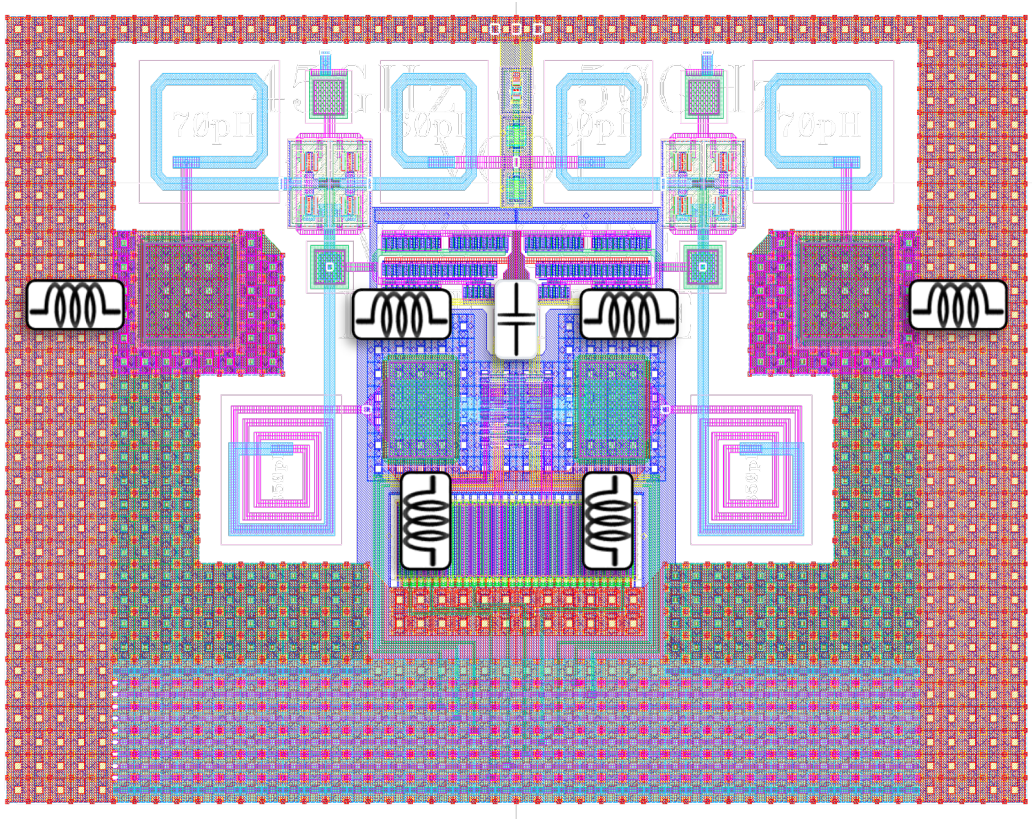
VCO Final Layout Example



- Notice the schematic & layout have similar component placement!
  - This technique is very helpful in optimizing the final layout at the schematic design stage
- Many of the previous LNA design techniques can be also be found in this layout
- Note the left/right symmetry of both the schematic & layout

VCO Layout Parasitic Implications

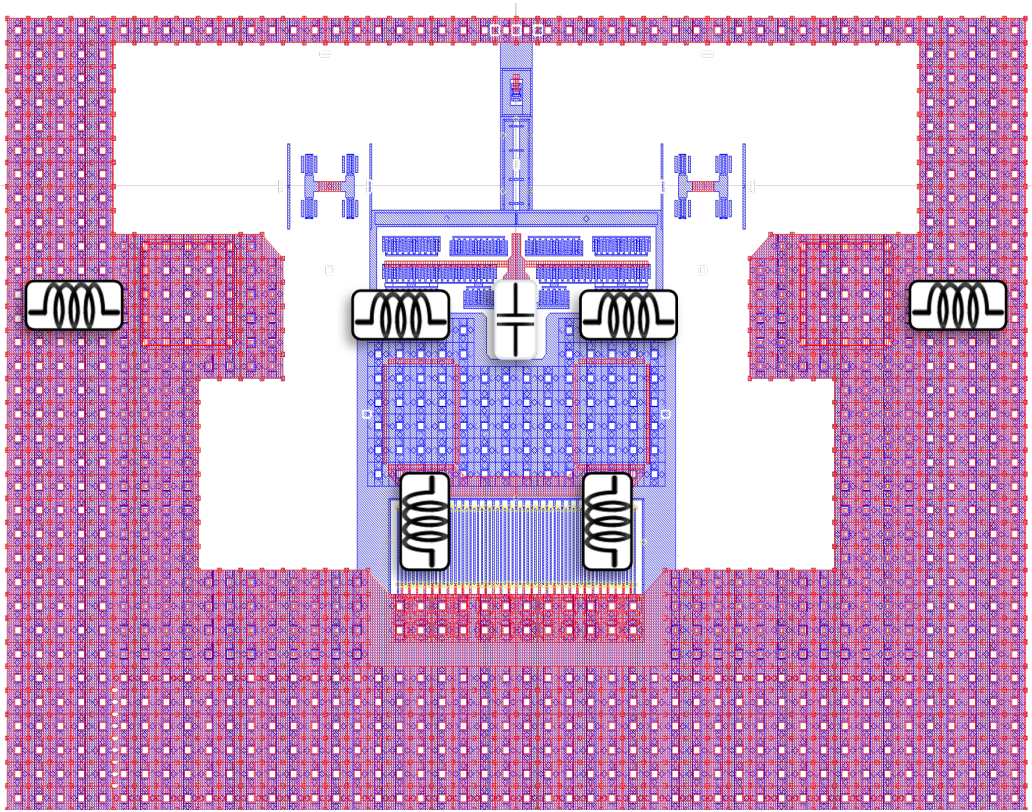
C M1 M2 M3 M4 M5 M6 M7



- Impact of top-level parasitics on VCO center frequency can be significant
- Focus on parasitics with the highest influence on VCO frequency
  - VCO tank interfaces to the top-level layout layers such as GND, VDD & biasing nodes

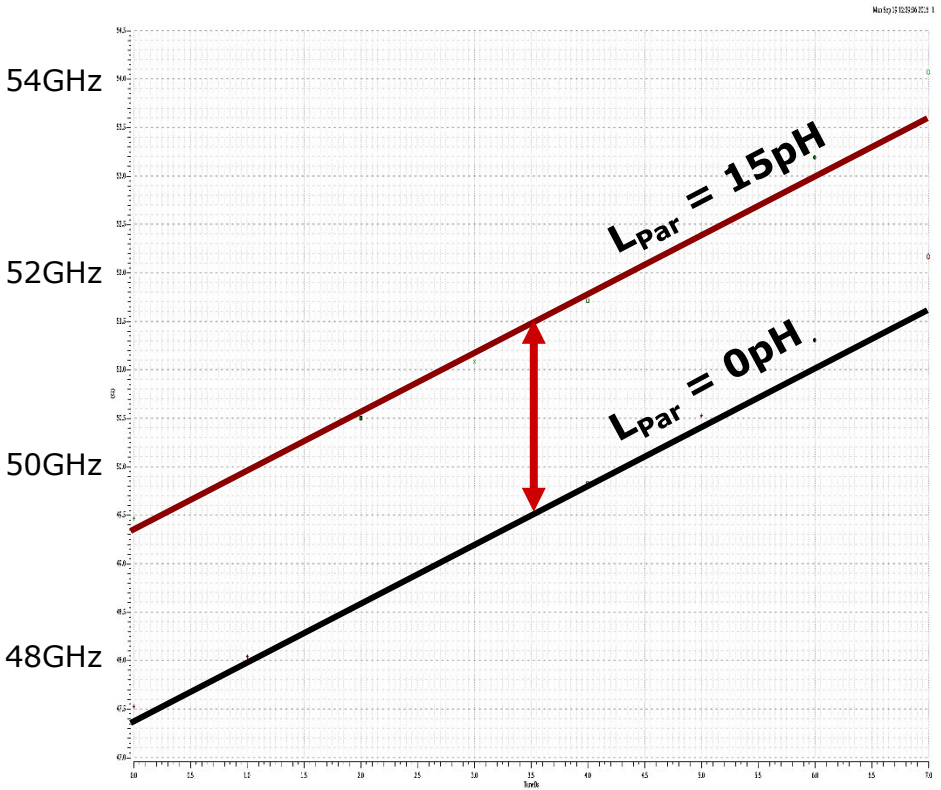
VCO Layout Top-Level EM Extraction

C M1 M2 M3 M4 M5 M6 M7



- Top-level EM extraction including all layers is time & computationally intensive
  - Iterations on layout also become more difficult
- Typically, top-level EM extractions are reserved for final verification only and not during design cycles

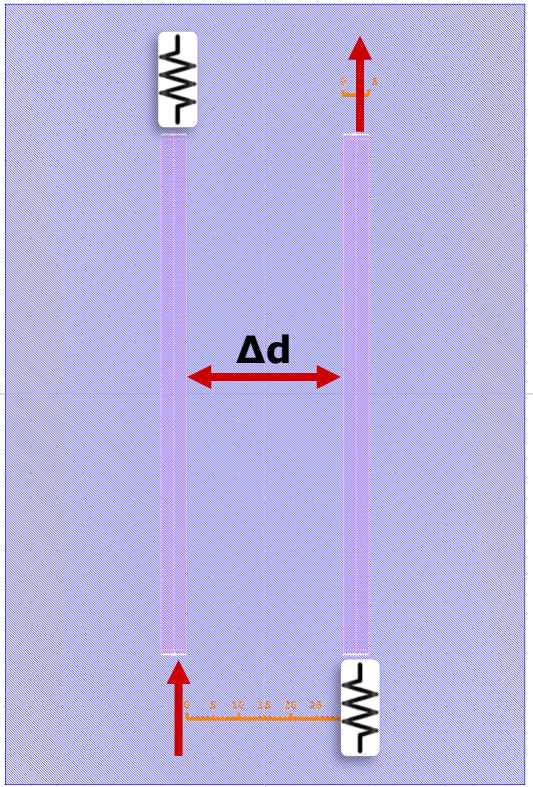
VCO Center Frequency Simulation



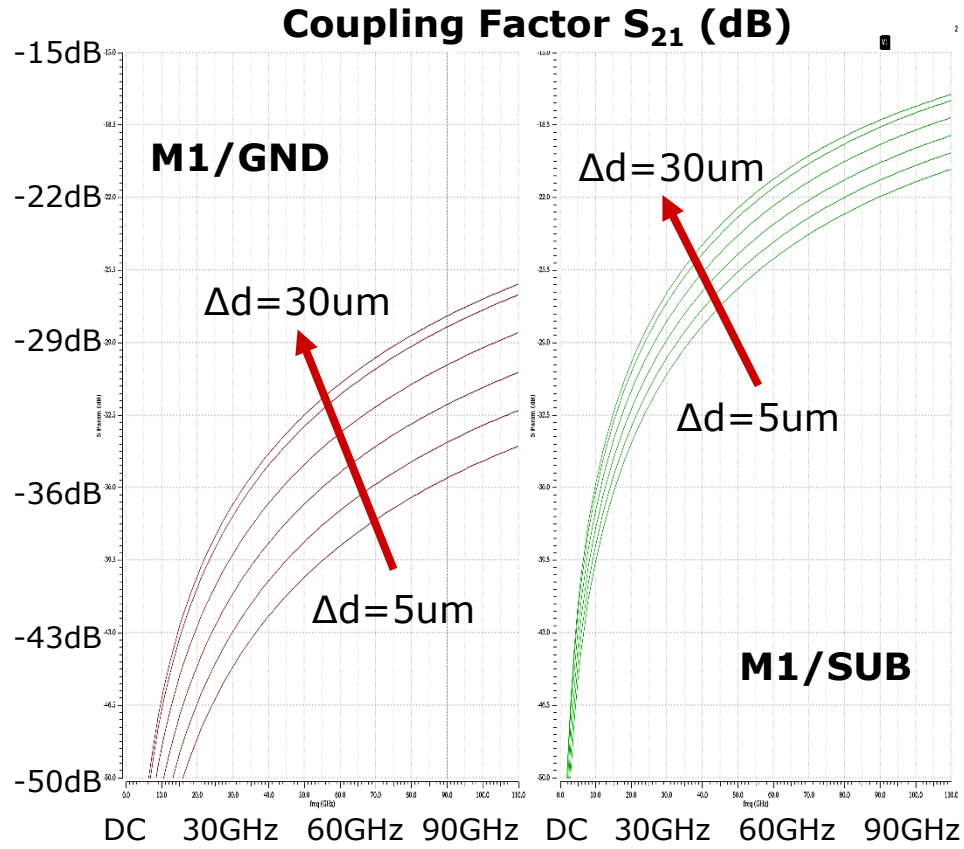
- L_{Par} represents the parasitic inductance to the VDD plane from the VCO load inductances
  - Due to the inductor placement, it is not possible to fully eliminate L_{Par}
- Similar behavior can be observed from all other parasitics affecting the VCO tank core

Undesired Coupling & Crosstalk

- Undesired coupling is inevitable & varies widely depending on the BEOL and layout techniques
- In RF application interactions between LO, IF & RF lines can have detrimental effects
- Multi-lane transceivers also suffer from cross-talk problems due to coupling both on-chip and off-chip
- Not all coupling is bad. Coupled lines have a wide range of applications

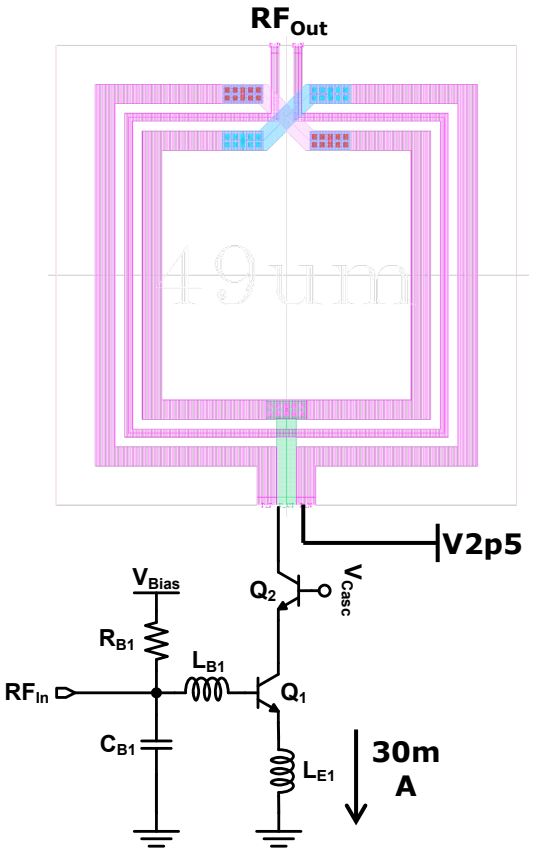


Coupled-lines Simulations



- The strength (& phase) of coupling depends on a lot of factors
  - Interconnect dimensions, distance, GND planes, proximity effects, aspect ratios, loading, etc.
- Coupling is (mostly) due to a combination of magnetic & capacitive effects
- Substrate modes and leakage also play an important role (see later)

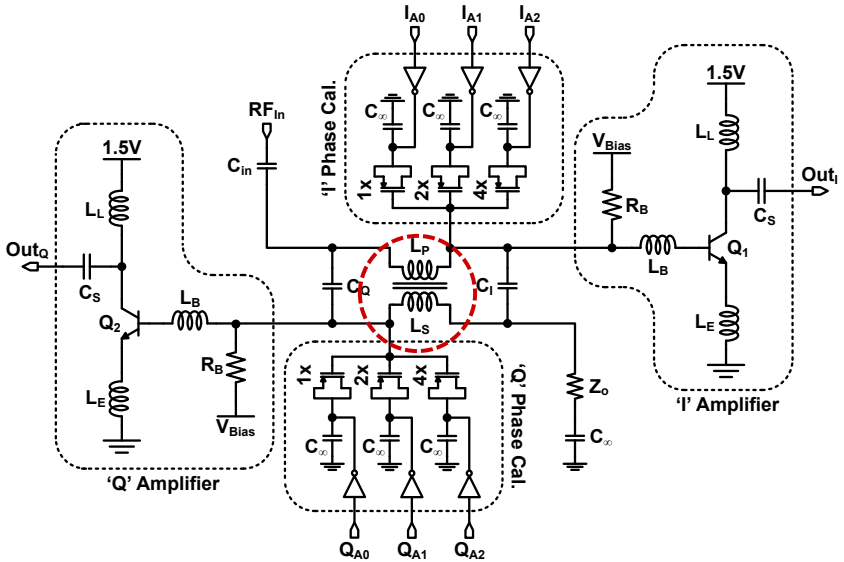
Other Limitations of Monolithic Passives

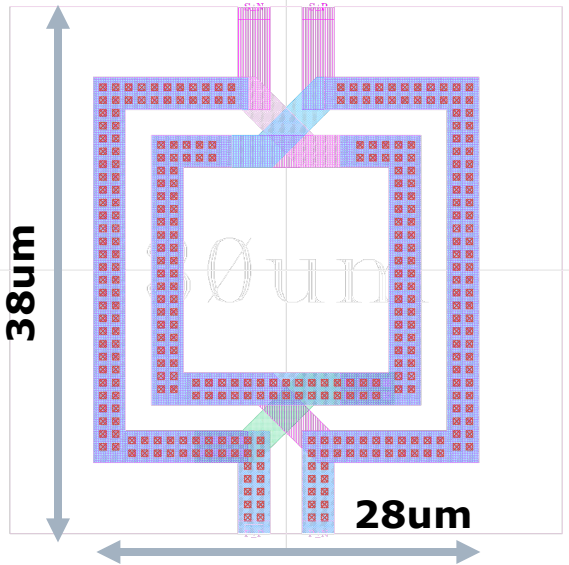


- Circuit on the left uses a balun to convert the single-ended collector RF current of transistor Q_2 into a differential signal output at RF_{Out}
- Inductors, transformers and interconnects can yield desirable performance electromagnetically and satisfy DRC rules while still be non-implementable due to electromigration limitations and even catastrophic failures
- Copper BEOL offer significant advantage over Aluminum regarding electromigration rules especially at higher temperatures

To Lump or not to Lump! (Example 1)

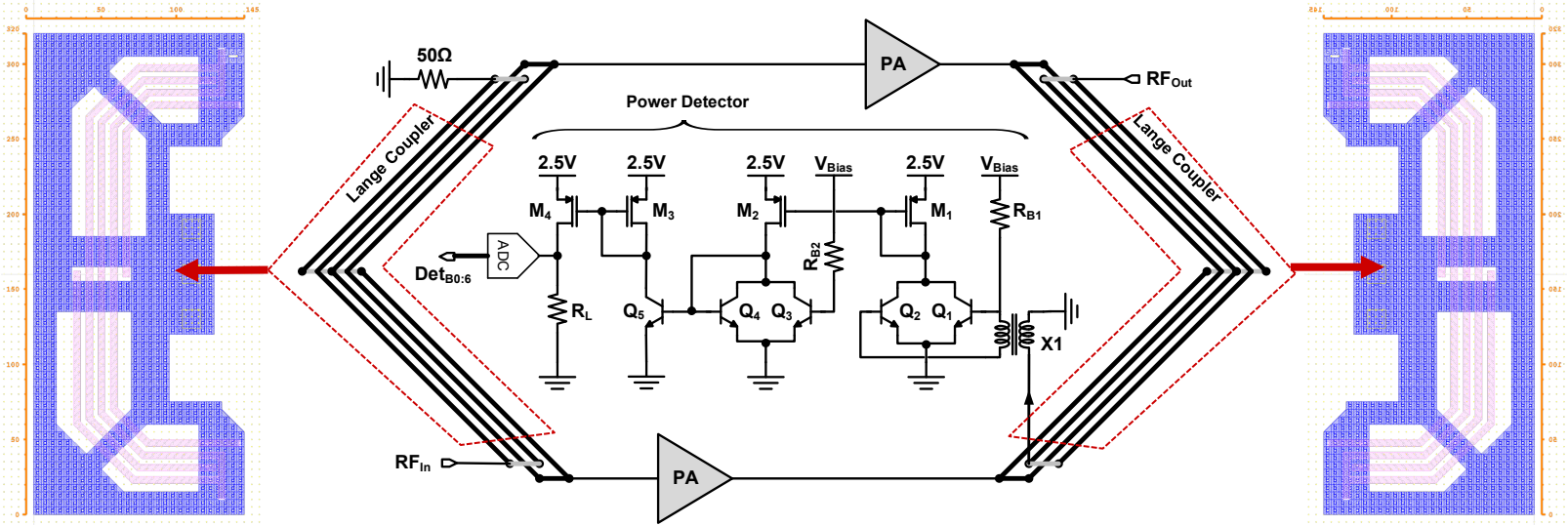
C M1 M2 M3 M4 M5 M6 M7





- W-Band I/Q generator at the heart of a phased array element vector modulator (phase shifter). Grows with the number of elements!
- The size of this block is critical & input/output access should be in close proximity. A lumped transformer is therefore preferred despite having higher losses

To Lump or not to Lump! (Example 2)

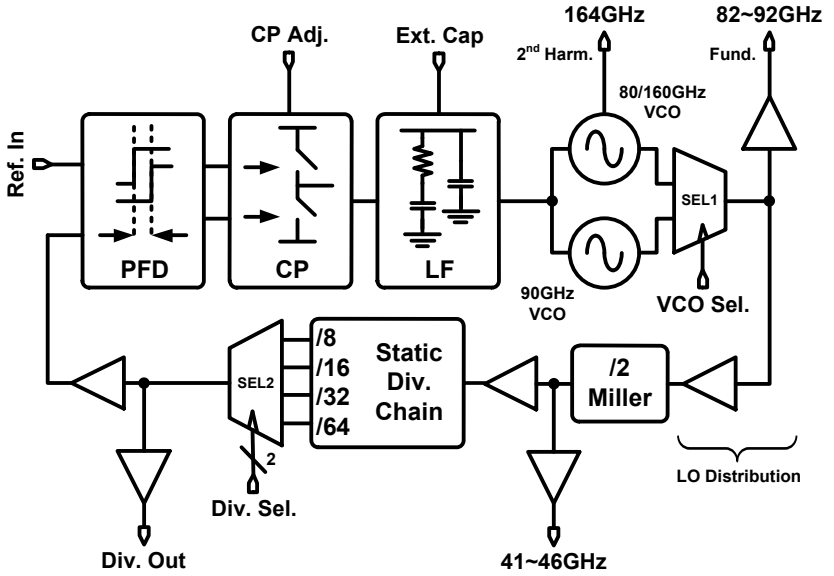


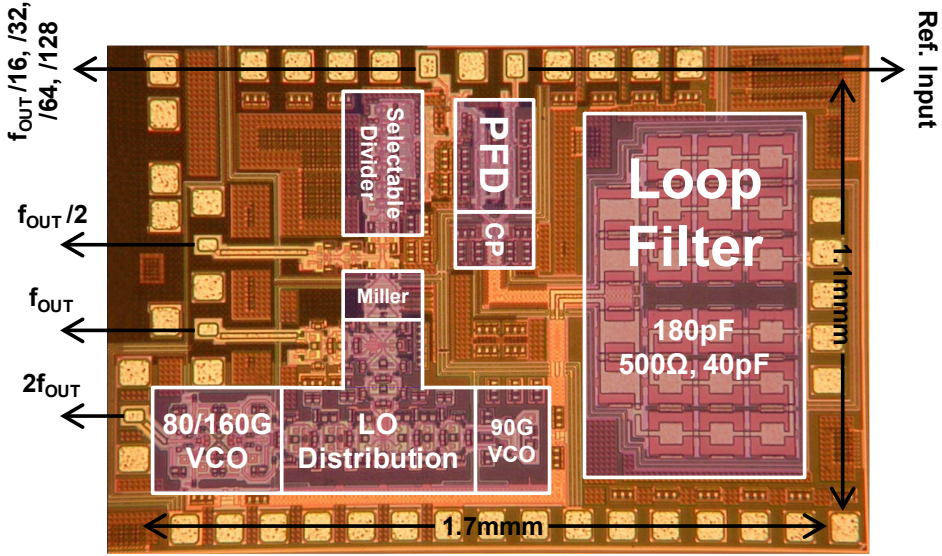
- W-Band balanced PA (with fault detector) as part of a transmitter phased array element
- Despite its larger size, a Lange coupler (with a folded layout structure) is used to maintain a reasonable PA efficiency. In this case, a lumped structure is not preferred

Large System Design Considerations & Examples

- Everything gets harder!
- Physical distance between blocks makes mm-wave passives more difficult to implement
- Isolation degrades, power supply rejection becomes more difficult
  - Requires careful distributed decoupling networks
- Layout placement is even more critical in overall system performance
- Co-design of integrated circuits, multi-chip systems and packaging is now common practice in nearly every domain
- Designers must be more coordinated, more communication is required
  - Can’t offload top-level layout assembly to inexperienced designers

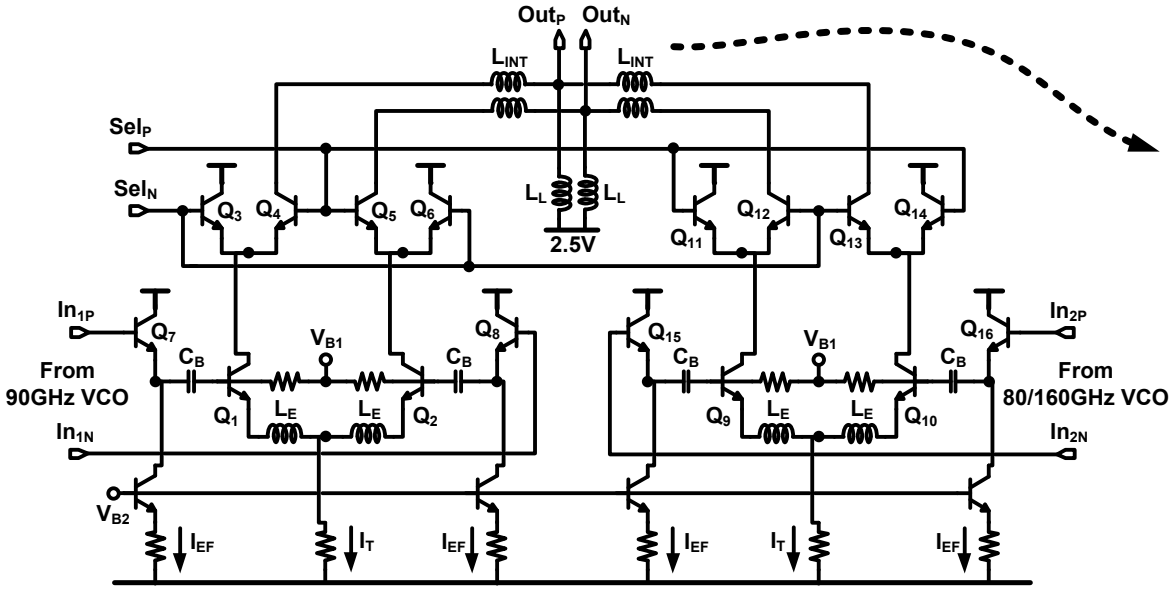
Mm-Wave/D-Band PLL Block Diagram

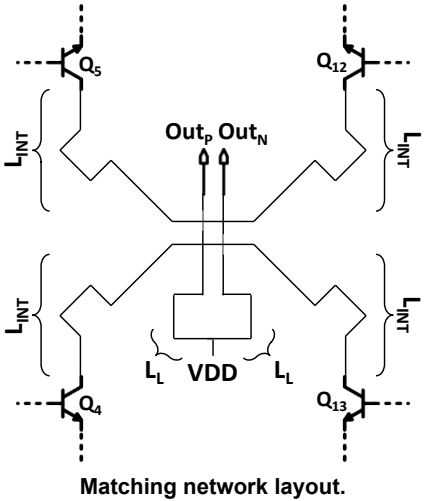




- Mm-Wave PLLs demand exceptionally careful layout and floorplanning due to the combination of high-frequency, low-noise, mixed-signal & presence of high-dynamic range signals throughout the IC
- How do we isolate the sensitive analog-loop signals (such as charge-pump, VCO tune, etc.) from the rest of the high-power signals?

VCO Selector Layout Considerations

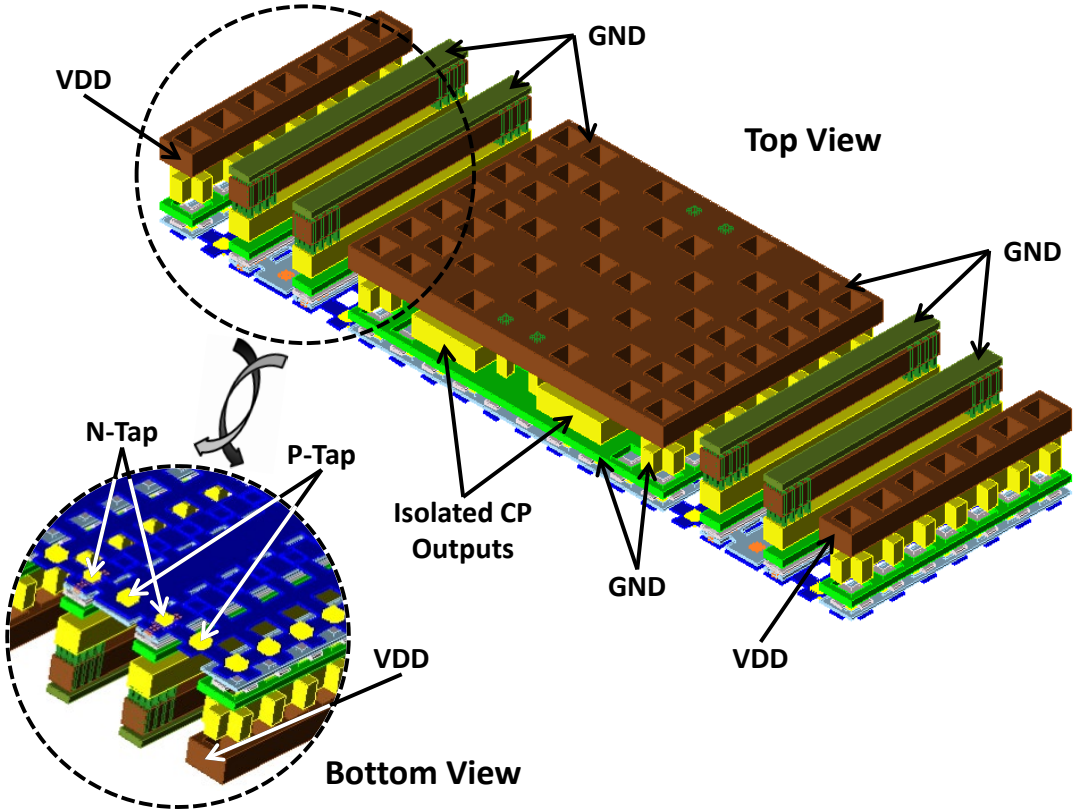




Matching network layout.

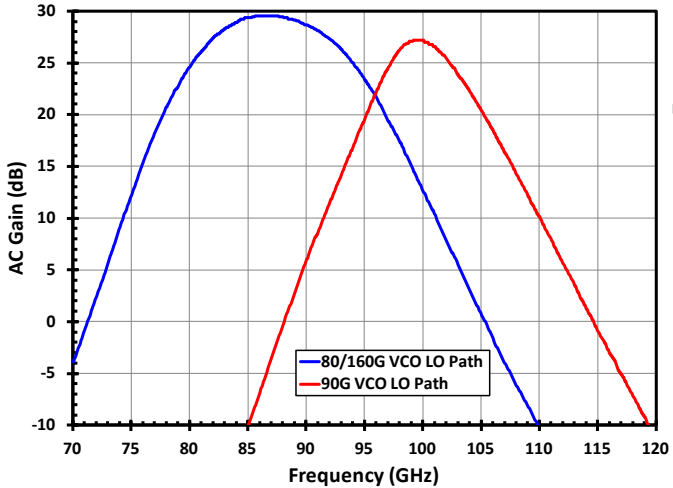
- Mm-wave block interconnects force us to be creative with layout placement and passive element realization
- Unavoidable interconnect parasitics may have to be absorbed into various matching networks in an iterative top-level floorplanning

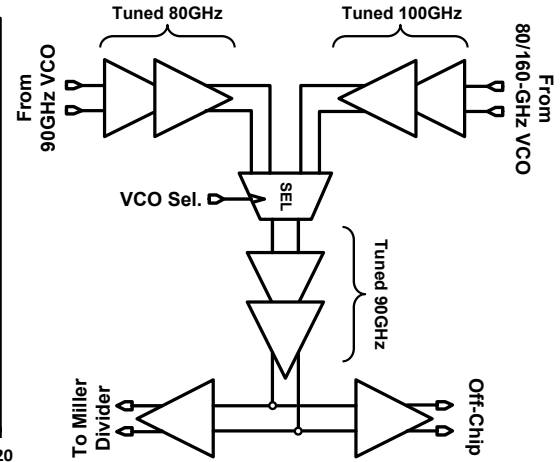
On-Chip Isolation Structures

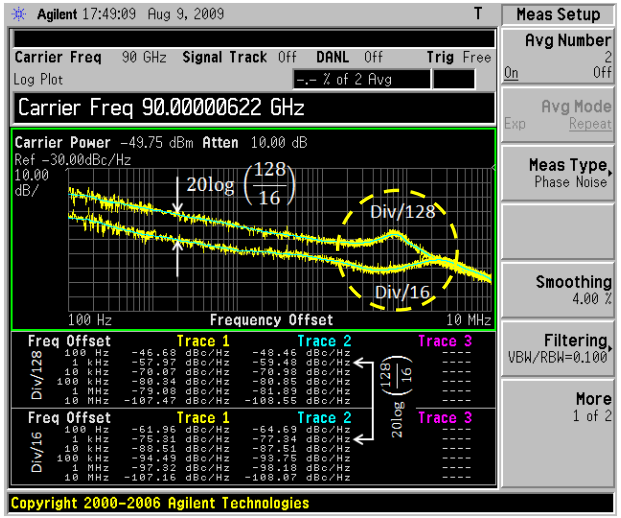


- Clever use of BEOL mesh blocks can be used to create mini-Faraday cages on-chip
- Alternating N-Tap & P-Tap substrate contacts can disrupt undesired coupling & substrate propagation
- Scalable mesh design simplifies layout both locally and globally for floorplanning

PLL Clock Distribution & Phase Noise Performance

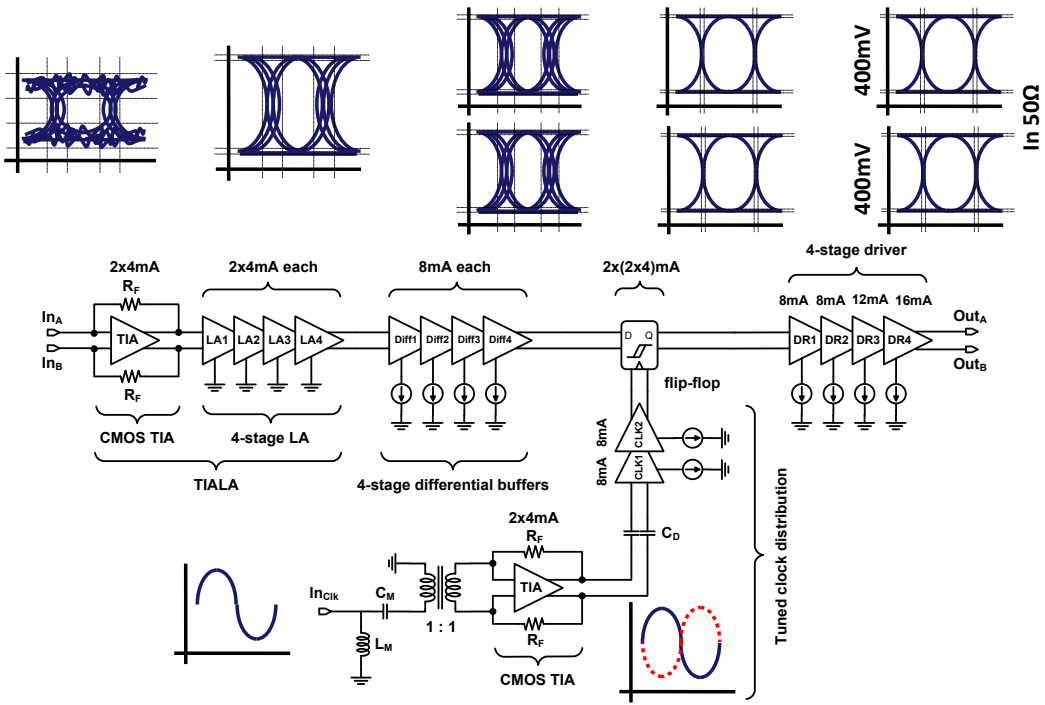






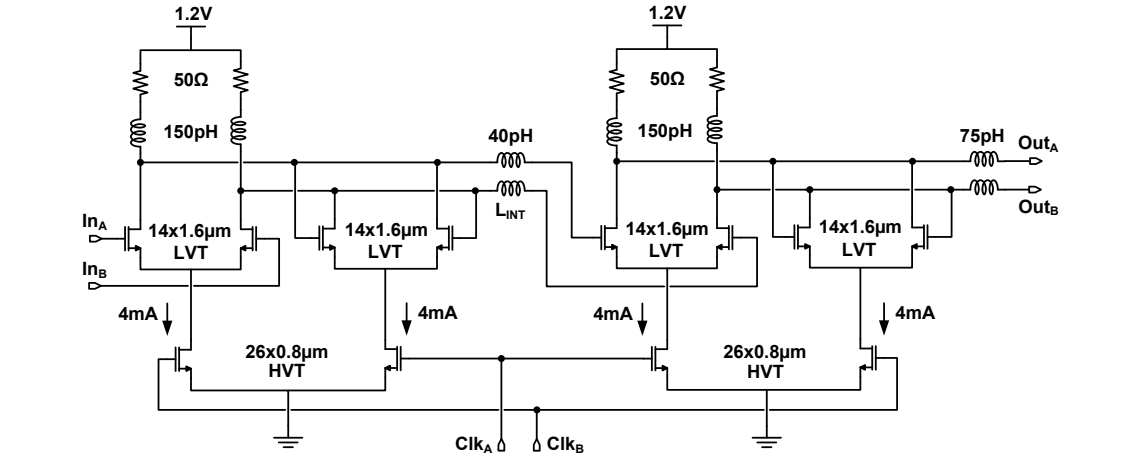
- Consider the difference between large-signal and small-signal behavior of a chain of amplifiers on isolation requirements on-chip
- Distributed and lumped elements have vastly different effects on substrate signal injection. This is true for single-ended versus differential implementations as well

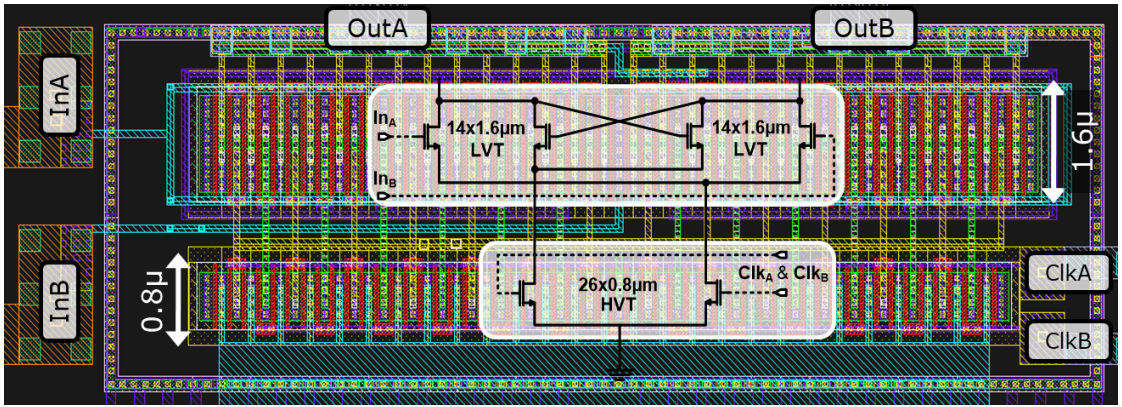
81Gb/s TIALA Retimer Block Diagram 65nm CMOS



- Mm-wave broadband circuits such as SerDes, TIAs, ADCs & DACs pose additional layout challenges
- Pseudo-differential and single-ended to differential conversion in broadband circuits is unique challenging
- DC coupled amplifier chains also require classic analog techniques

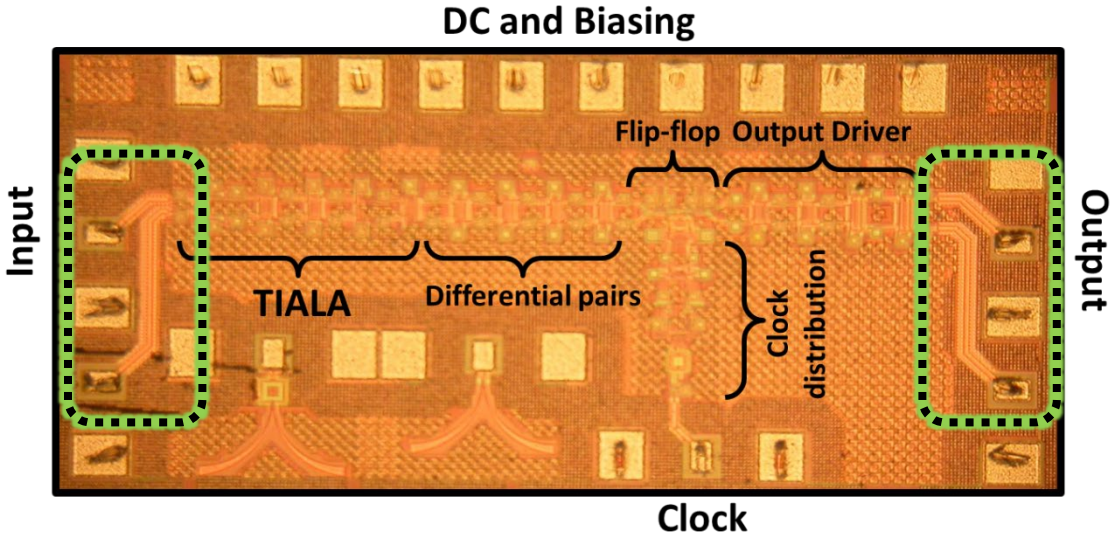
Pseudo-Differential Circuit Considerations

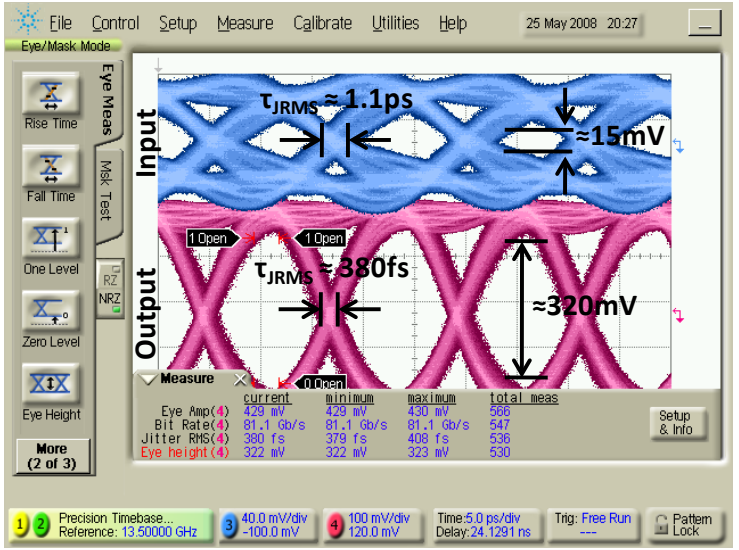




- Treat pseudo-differential GND and/or V_{DD} nodes carefully by joining the signals together before connecting them to the global GND/V_{DD} planes
- Notice the stair-case metal & via layout on CMOS source/drain nodes which reduces lateral coupling capacitances between transistor terminals

81Gb/s TIALA Retimer Die Photo & Performance

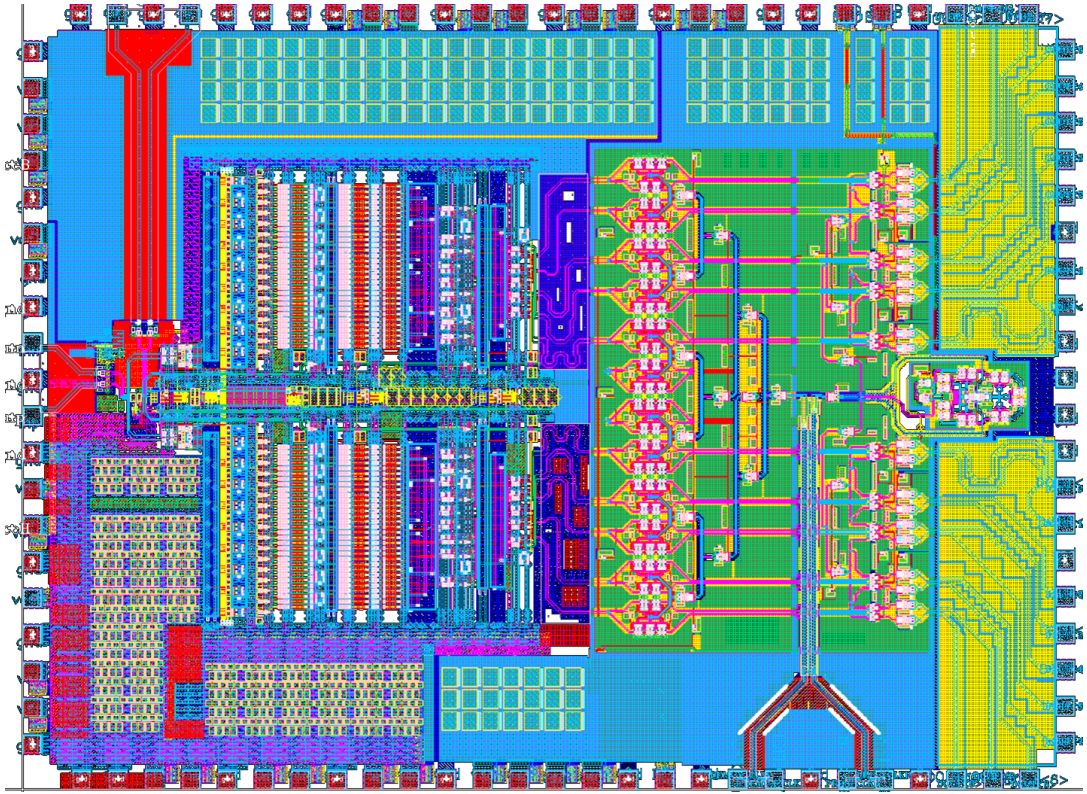




- Top-level layout offers differential input and output interfaces even though the input signal is single-ended
- What are the consequences of having un-equal transmission line lengths between the internal blocks and IC pads?

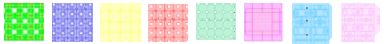
Top-Level Layout Problems (ADC)

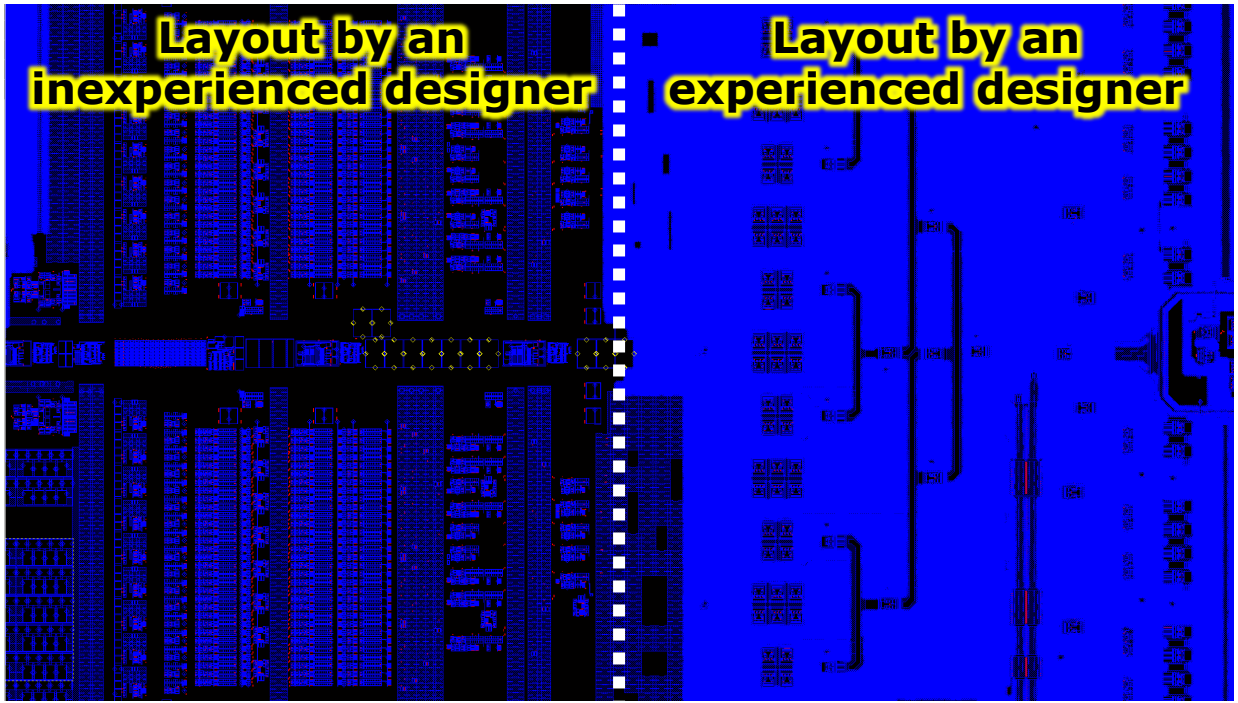
C M1 M2 M3 M4 M5 M6 M7



- Mm-Wave ADCs are particularly difficult to floorplan due to the sensitive mixed-signal and matching requirements
- Top-level layout of the IC with all layers visible may hide critical flaws!
- Let's take a closer look

Top-Level Layout Problems (ADC)

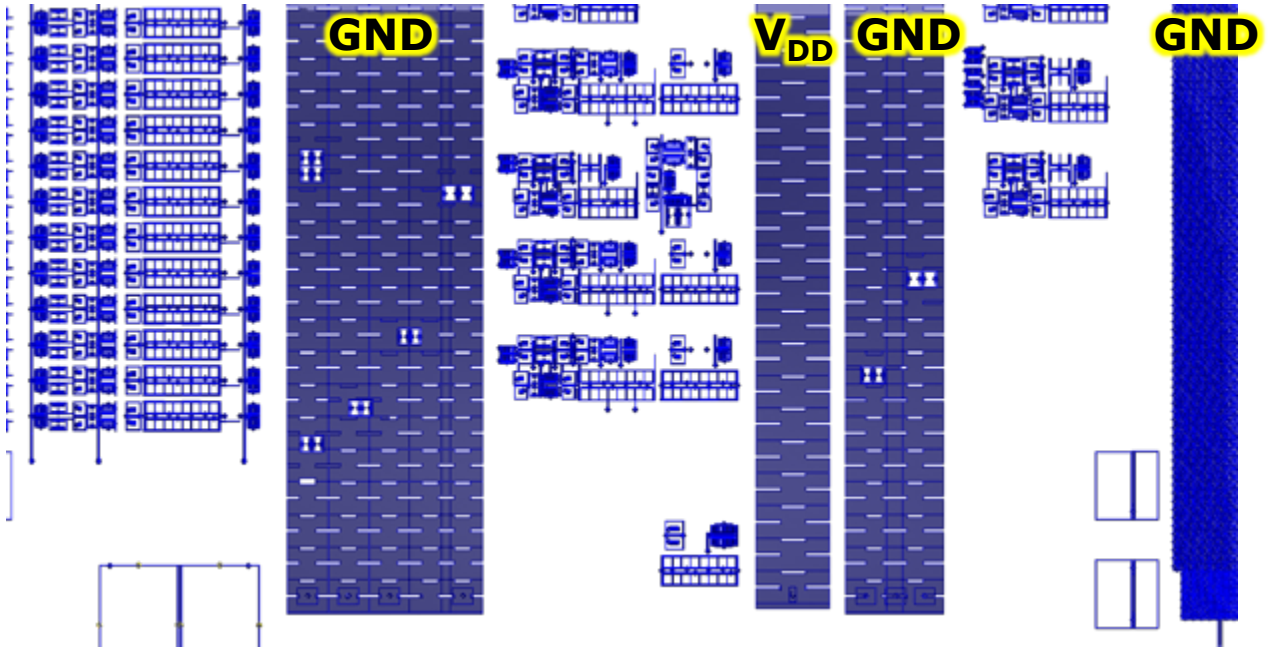




- Note the difference in GND plane distribution. The global GND plane must provide low DC resistance as well as low inductance. Highest density GND and VDD planes also offer distributed MoM capacitance

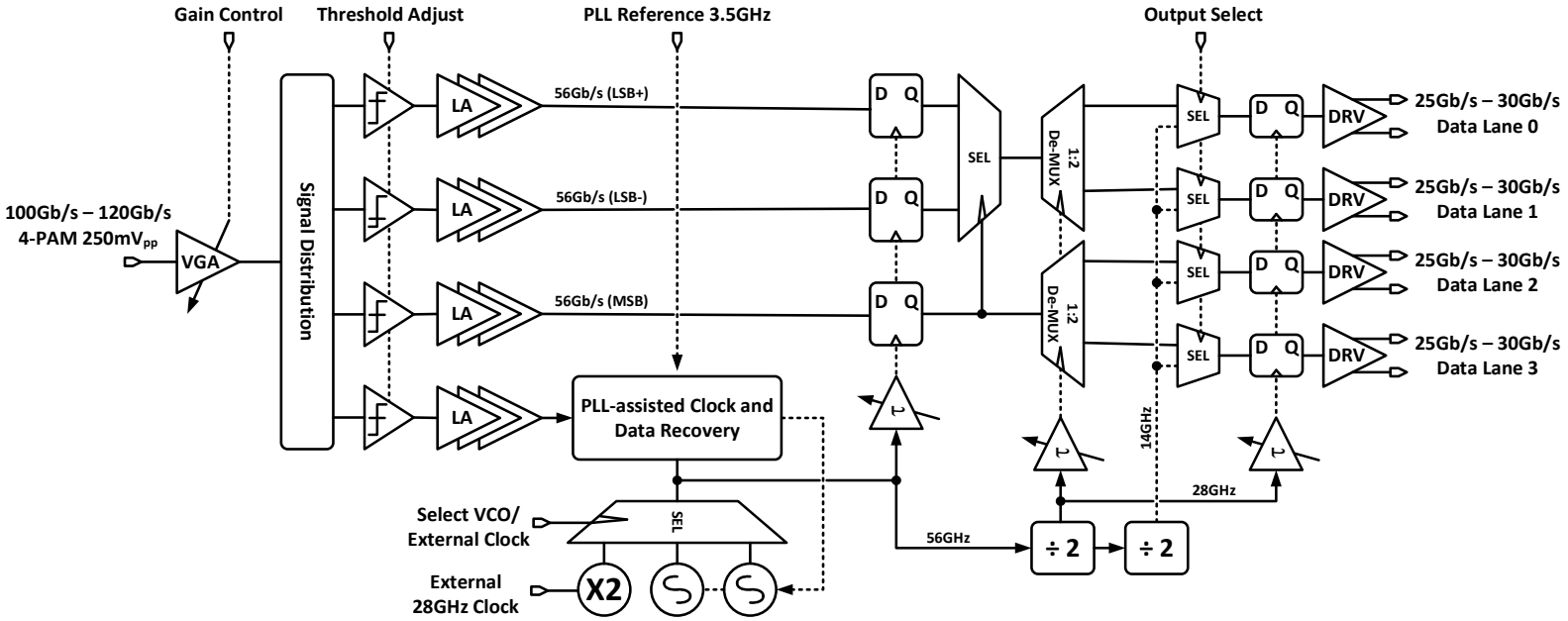
Top-Level Layout Problems (ADC)

C M1 M2 M3 M4 M5 M6 M7



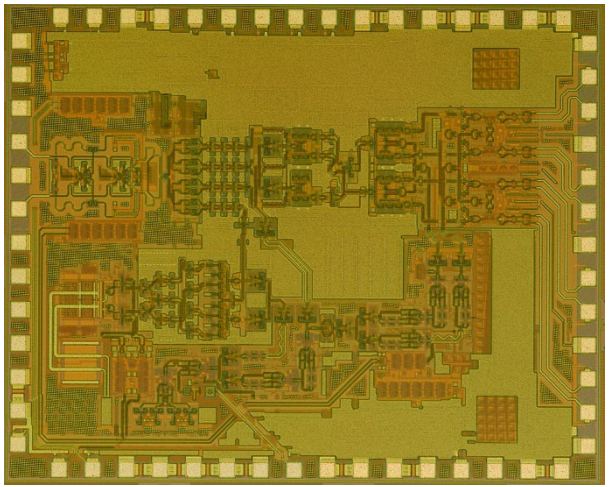
- Can you spot the fundamental flaw in the GND and VDD distribution bars?
- Note the direction of DC current flow and the metal slits which are required By DRC rules for local density requirements

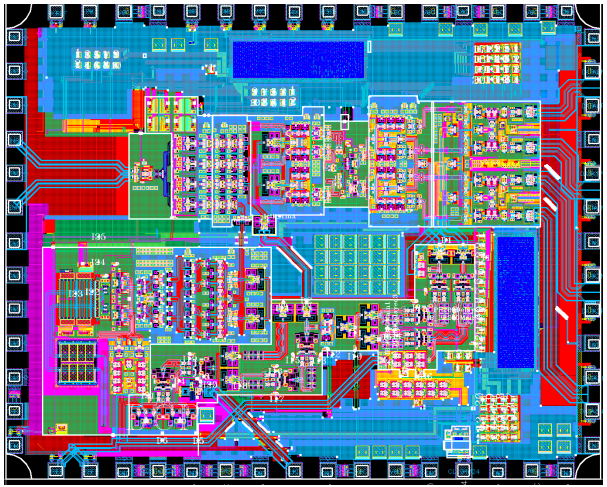
112Gbit/s 4-PAM Receiver IC (SiGe BiCMOS)

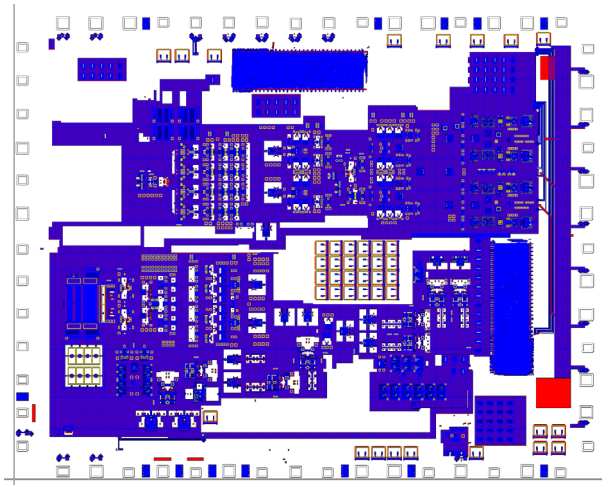


- Inclusion of a Clock & Data Recovery block on-chip requires careful isolation from broadband signal injection into the VCO & PFD
- Isolated islands of GND & V_{DD} planes are required

112Gbit/s 4-PAM Receiver Layout & Die Photo

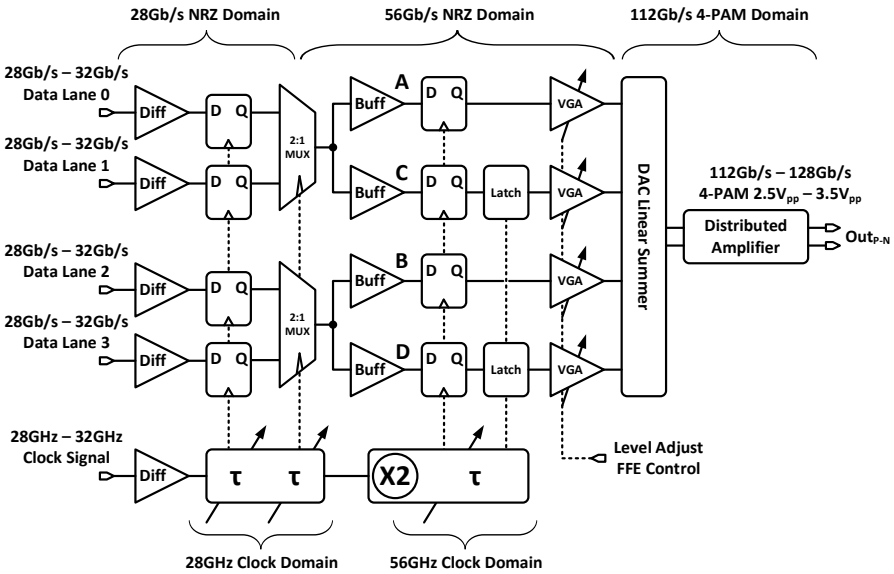


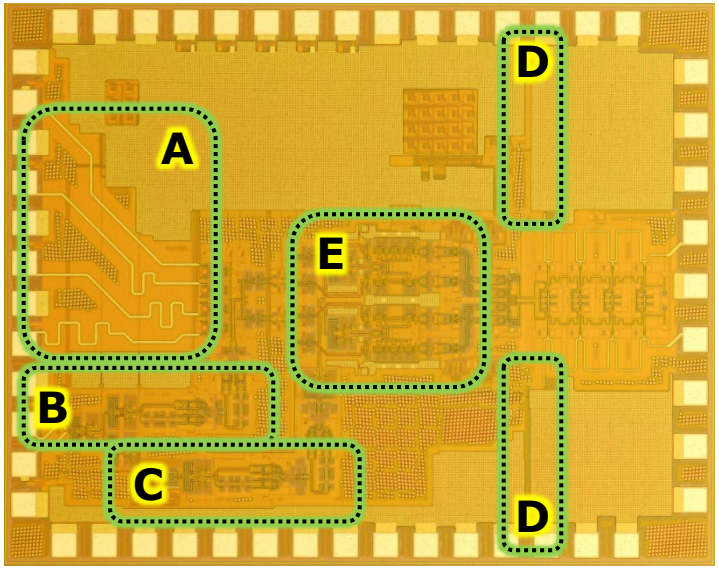




- Another example of identifying potential top-level metallization issues by examining each layer at the highest rendering visibility
- Note the placement of CDR core, demultiplexer and clock distribution networks

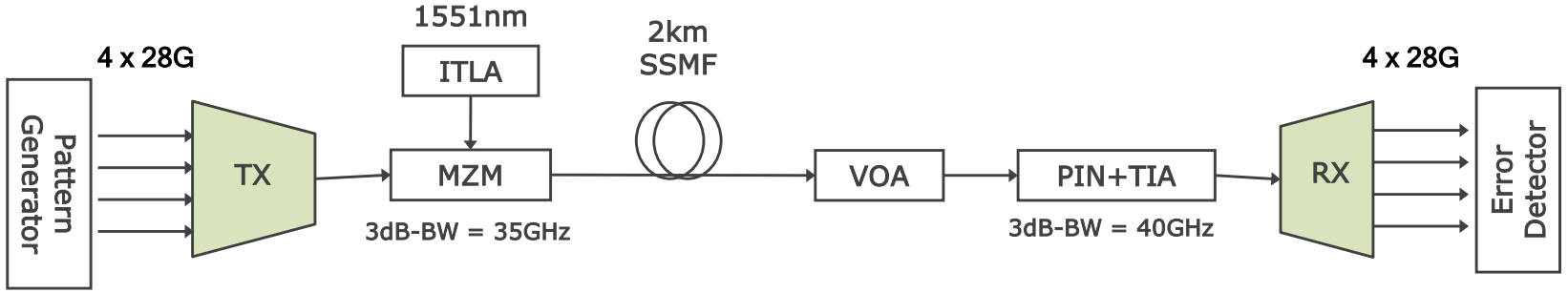
112Gbit/s 4-PAM Transmitter IC (SiGe BiCMOS)



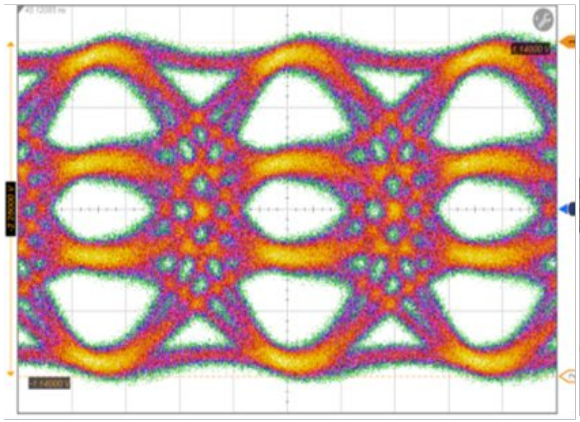


- A: Length-matched, single-ended NRZ inputs
- B/C: 28GHz & 56GHz clock domains (large signal isolation)
- D: Distributed amplifier power supply island for isolation
- E: NRZ to 4-PAM signaling transition and MUX

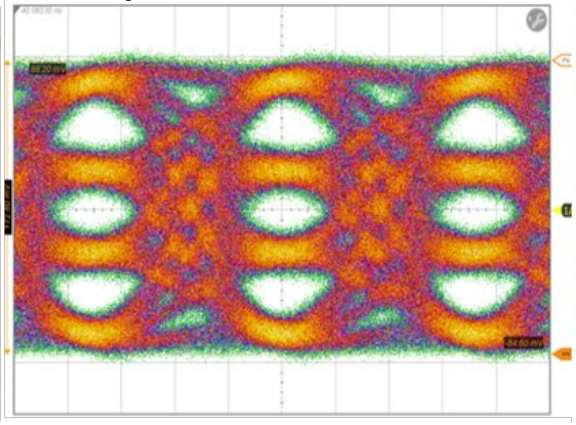
112Gbit/s Optical Link Measurements



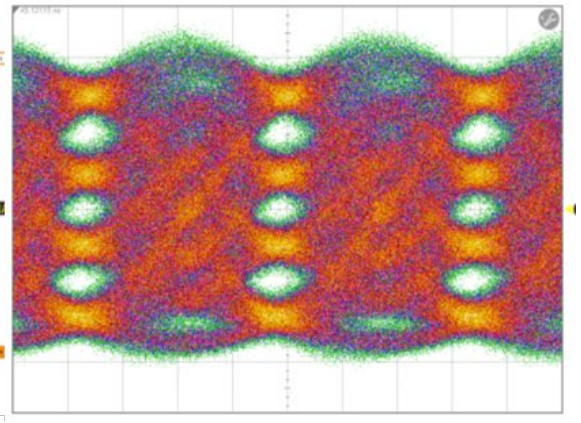
Electrical drive signal



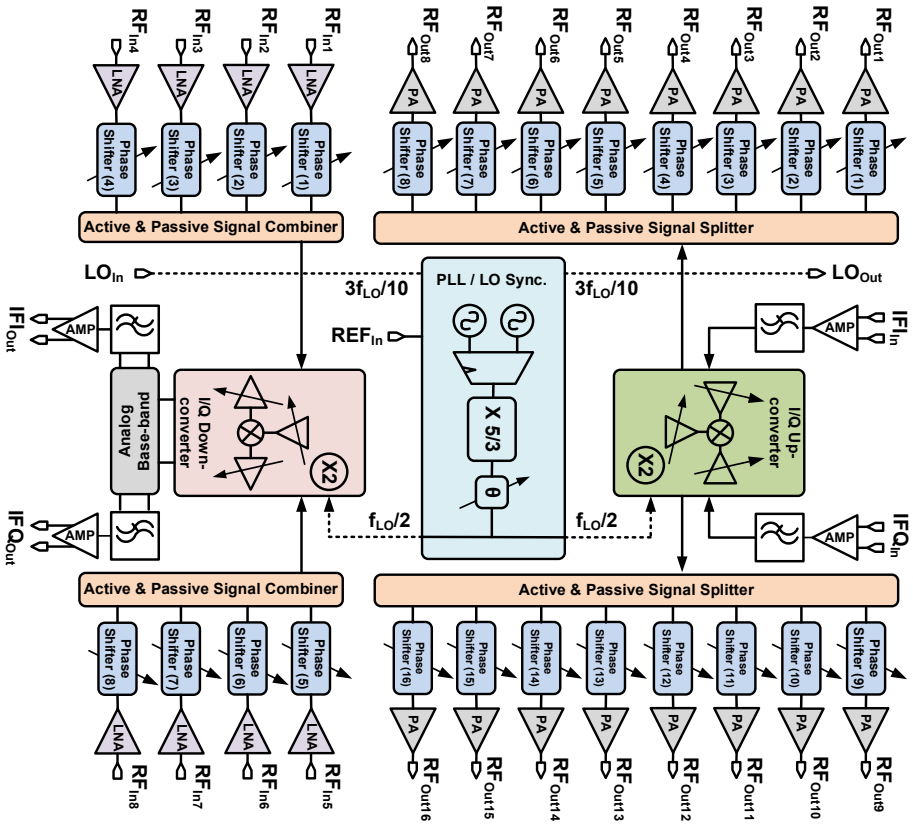
Optical back-to-back



Optical 2km SSMF



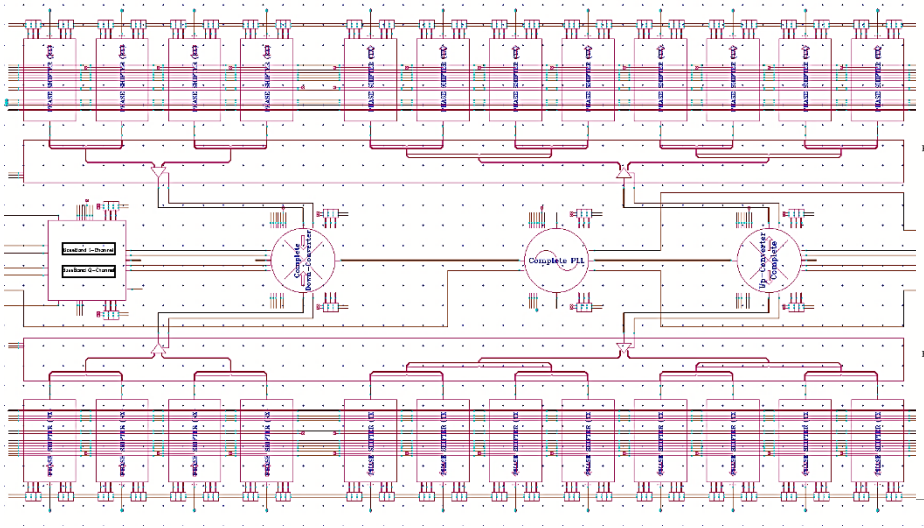
W-Band Phased Array Chipset Example

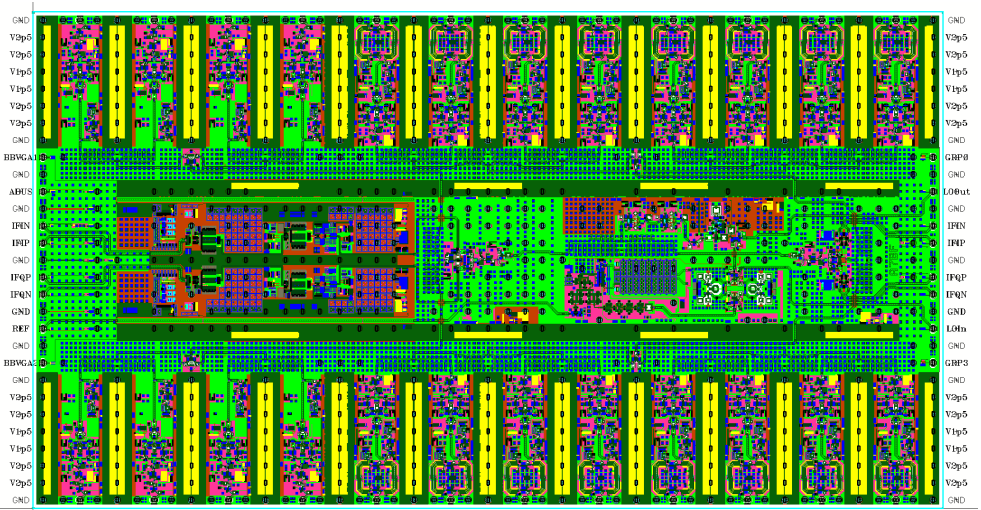


- Fully integrated 16-TX, 8-RX phased array chipset with built-in PLL, analog baseband, digital calibration & self-alignment
- Complex top-level layout due to space constraints as well as the co-integration of RF, PLL & digital signals on the same die
- How do we isolate the appropriate blocks and functions within the chip?

Top-Level Schematic & Layout

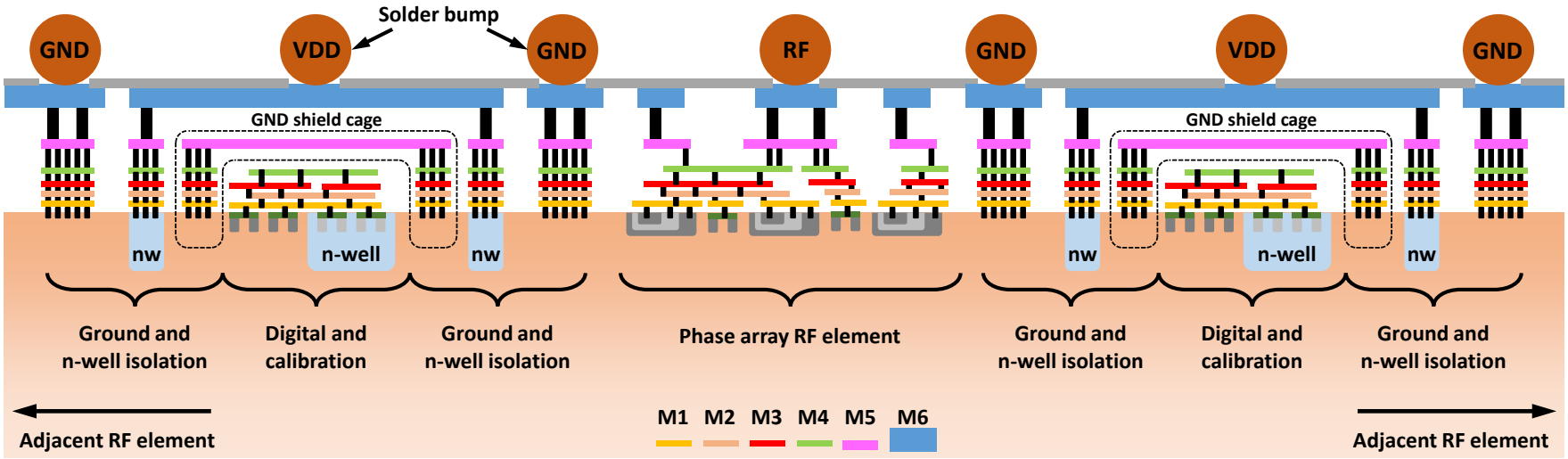
C M1 M2 M3 M4 M5 M6 M7





- Note the one-to-one placement of top-level blocks in the schematic view to the top-level layout floorplan
- This approach provides insight into interconnect and isolation requirements. It is simpler and more efficient to manipulate schematic view rather than layout view during floorplanning

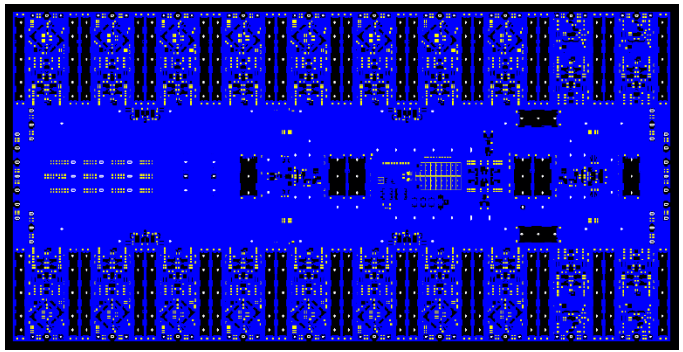
Isolation Techniques



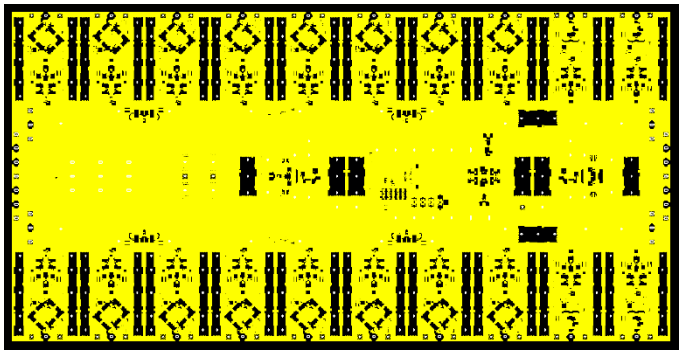
- Phased array element-to-element isolation as well as digital to RF isolation are critical especially in TDD scenarios
- Fully encapsulated CMOS sub-blocks shields digital activity from RF circuits
- Distributed CMOS memory reduces global digital routing to local routing
- Note that this layout technique is repeatable and scalable!

Phased Array Power & GND Distribution

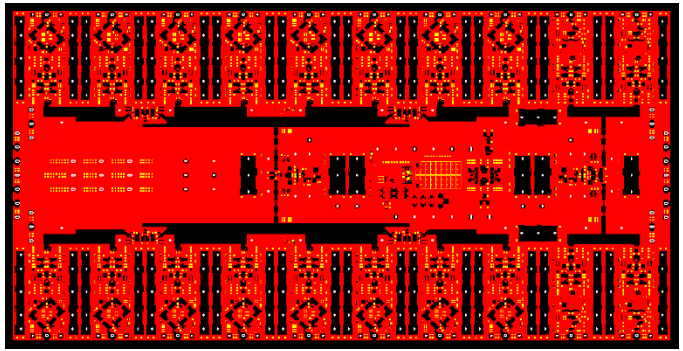
C M1 M2 M3 M4 M5 M6 M7



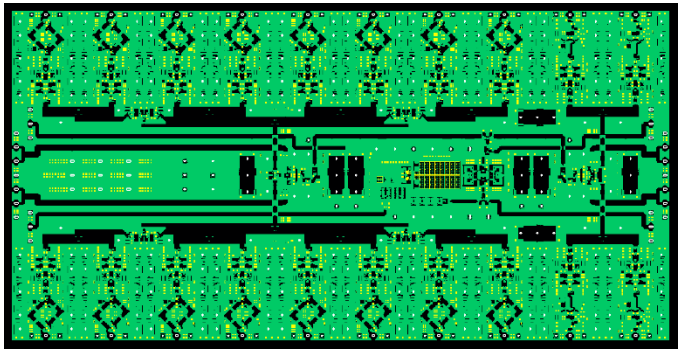
Metal 1



Metal 2

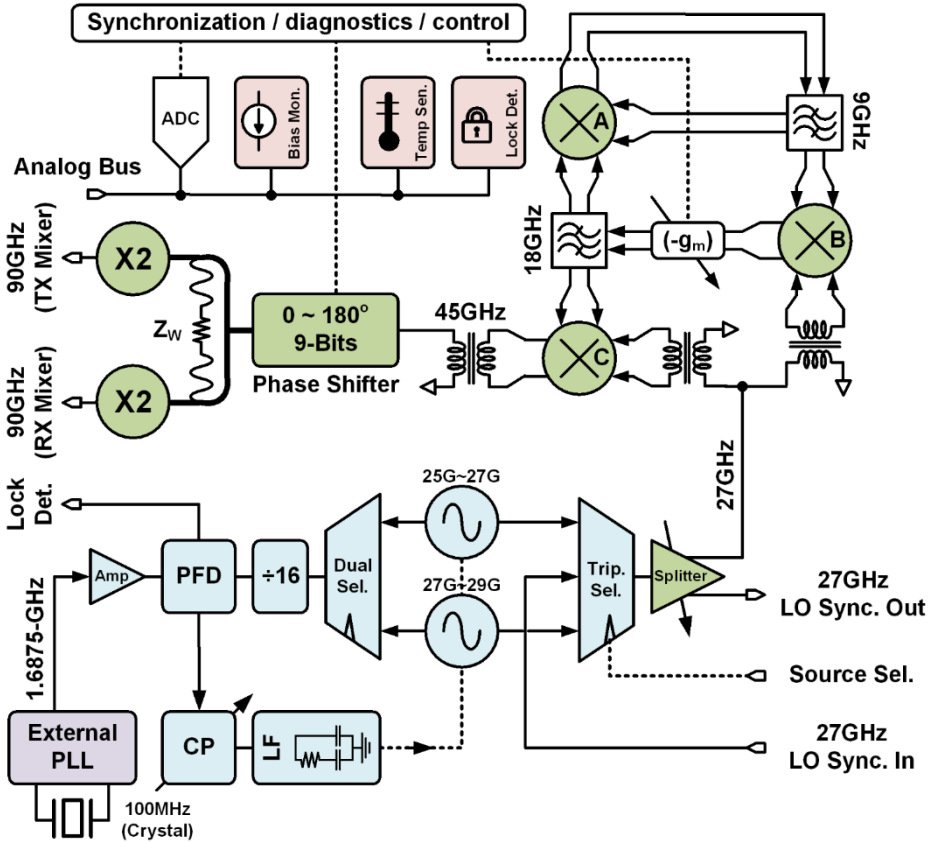


Metal 3



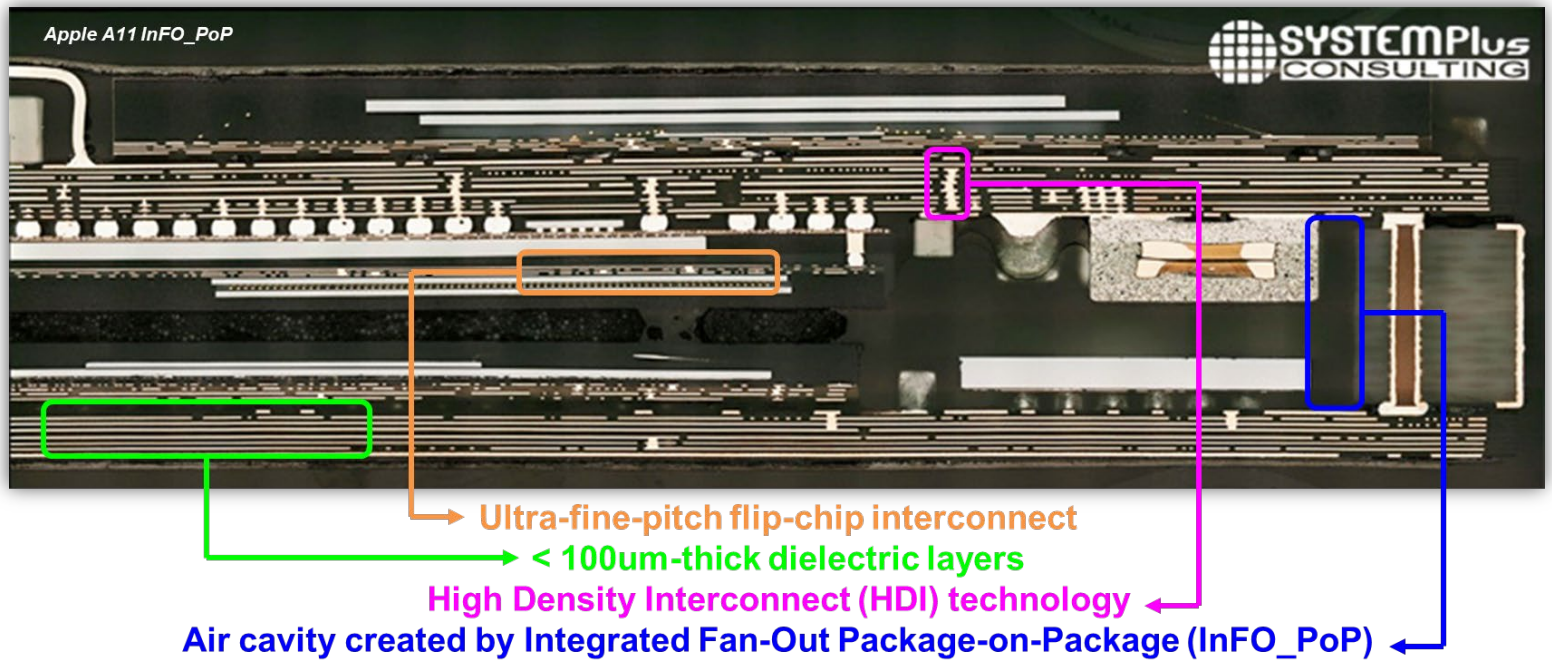
Metal 4

Isolation Limitations & PLL Architecture



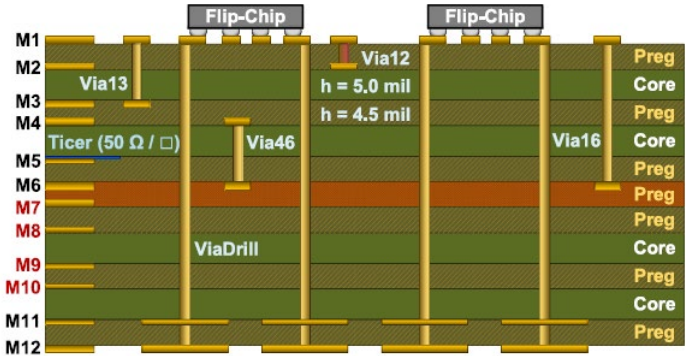
- In some situations, it may be impossible to achieve sufficient isolation between sensitive blocks on-chip
- The phased array PLL uses a prime ratio multiplier (5/3) to ensure the mixing terms between the RF PA outputs and VCO signal do not fall within the PLL bandwidth

“Moore’s Law” of PCBs

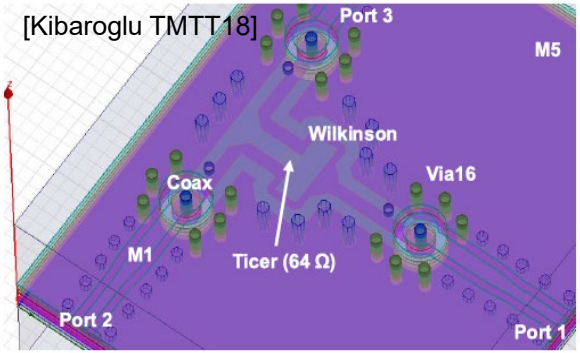


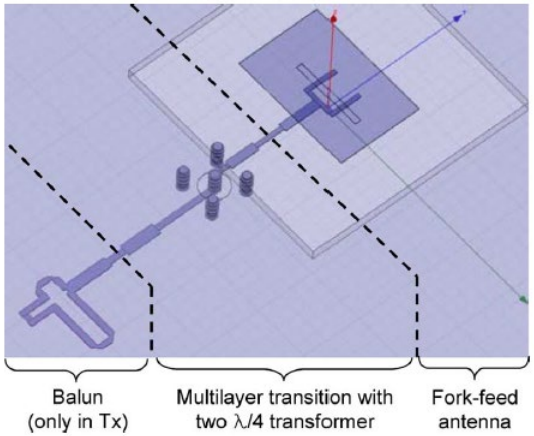
- Consumer products continue to push PCB technology and microelectronics packaging, in turn providing an excellent platform for mm-Wave

Via Transition Design in PCB

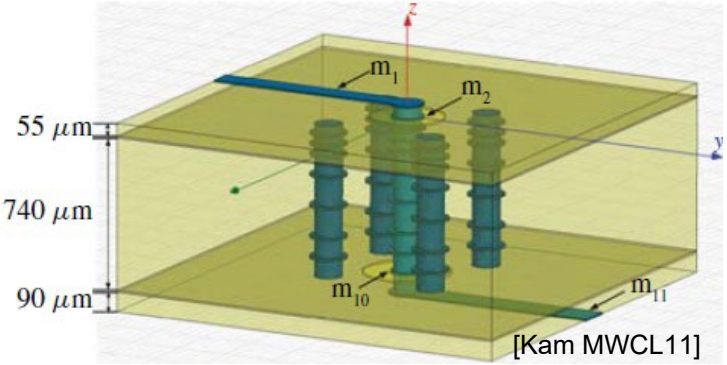


[Kibaroglu TMTT18]





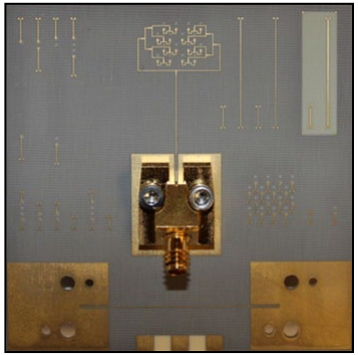
- No fundamental difference between a PCB stack and integrated circuit's BEOL!
- Lithography limitations, material properties and thicknesses force us to use PCBs differently and limit the maximum frequency of operation

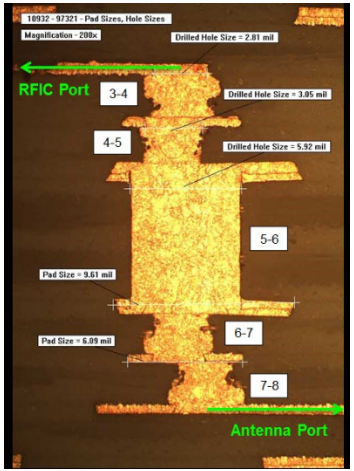


[Kam MWCL11]

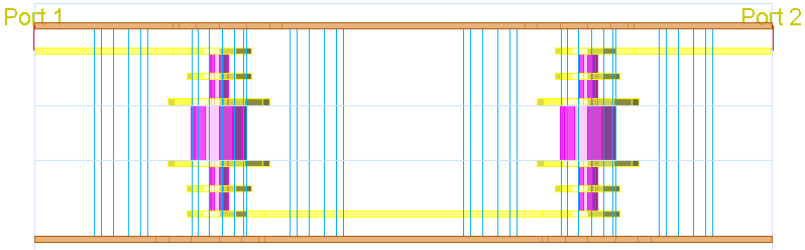
Pushing the Limits of PCBs

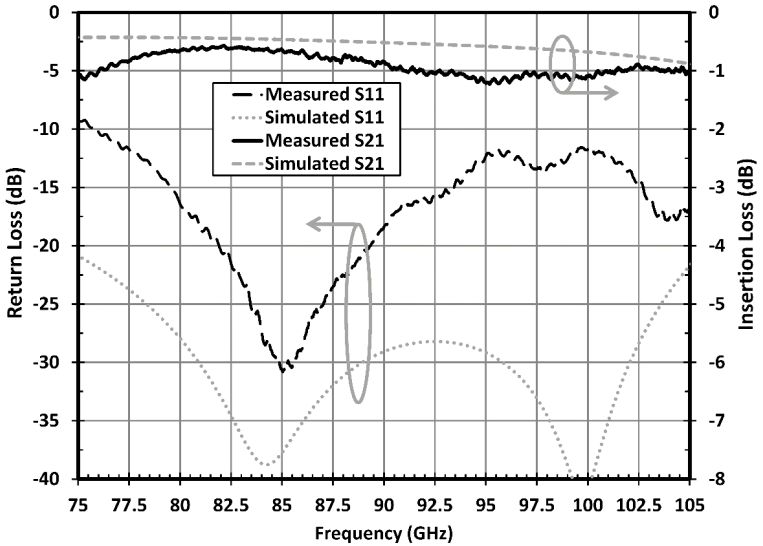
Organic Substrate





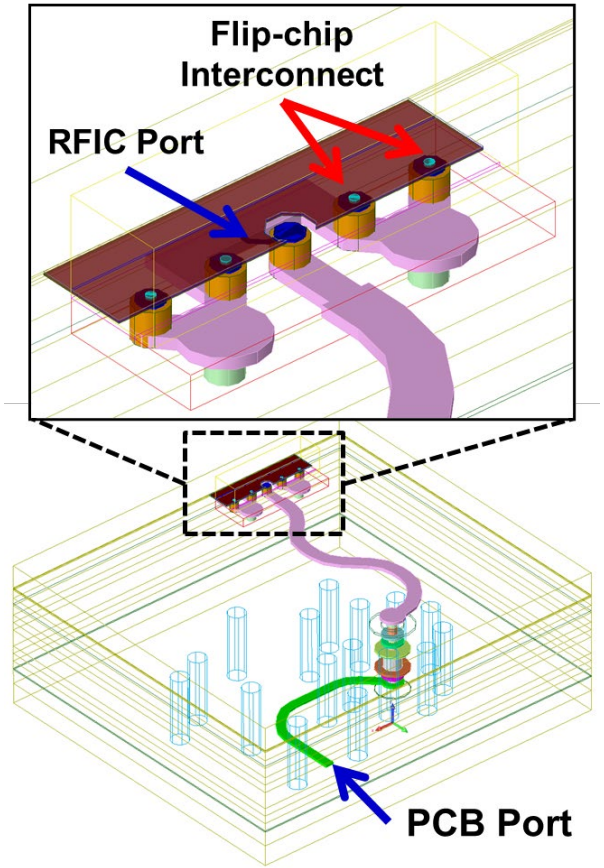
Back-to-Back Transition 3D FEM Model

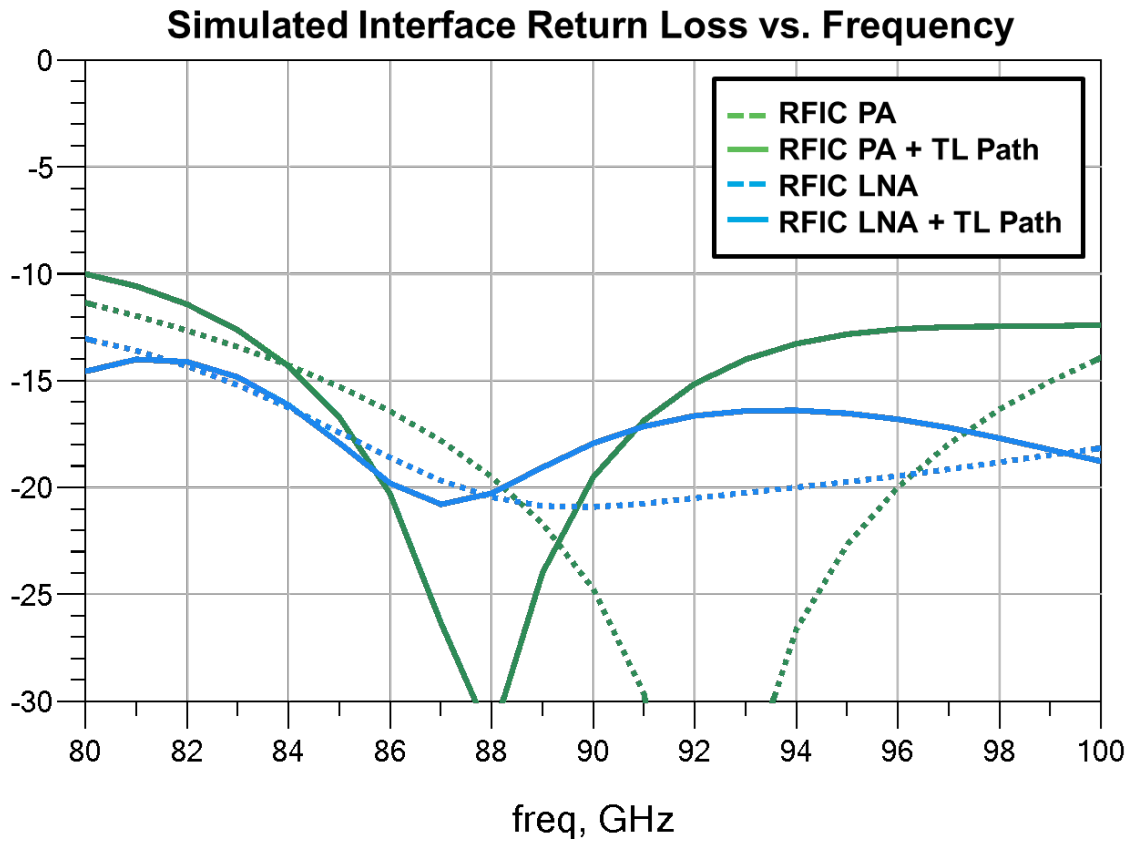




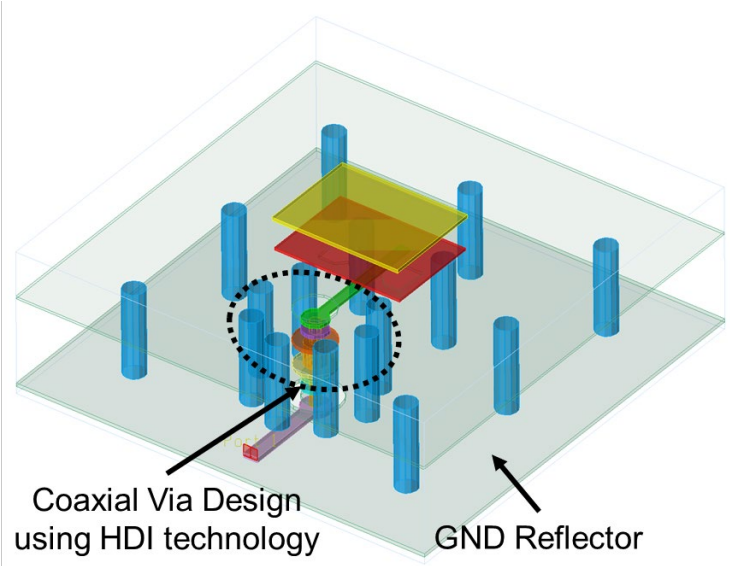
- Pushing the limits of PCB lithography enables direct W-Band flip-chip assembly
- Package-less integration combined with organic substrate offers low-cost solution even up to 110GHz
- How do we handle interfaces between IC & package?

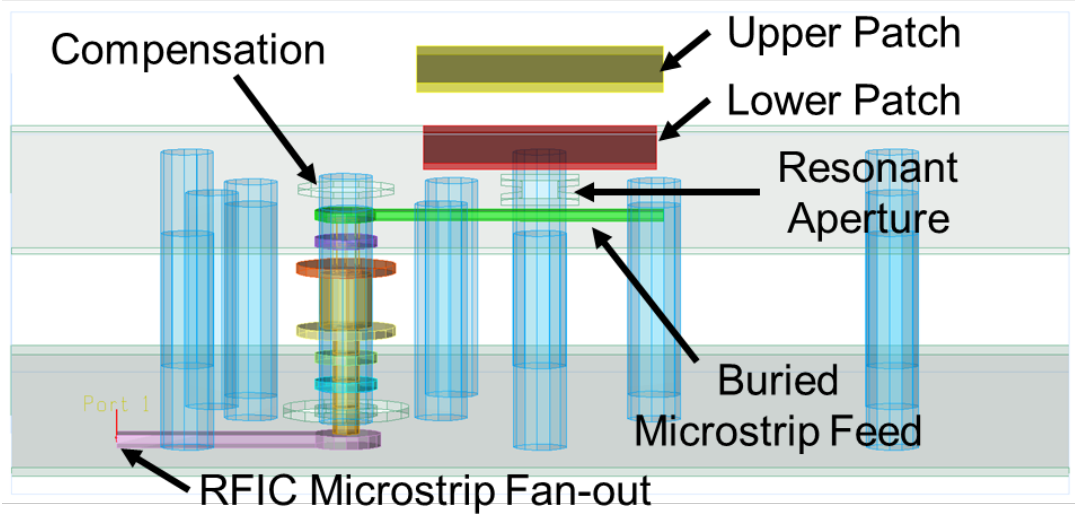
Mm-Wave Antennas as RFIC Extensions





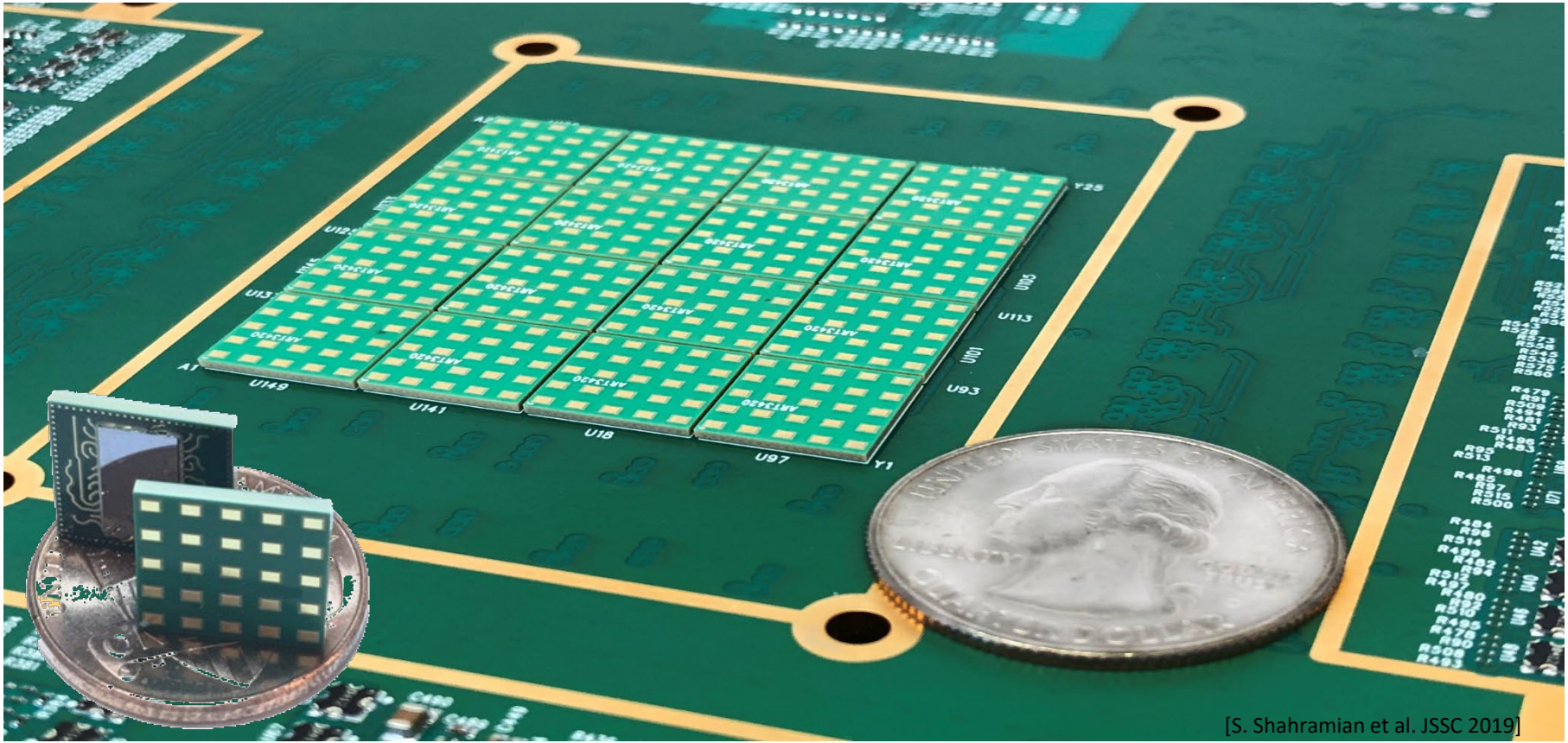
W-Band ASP Antenna Design





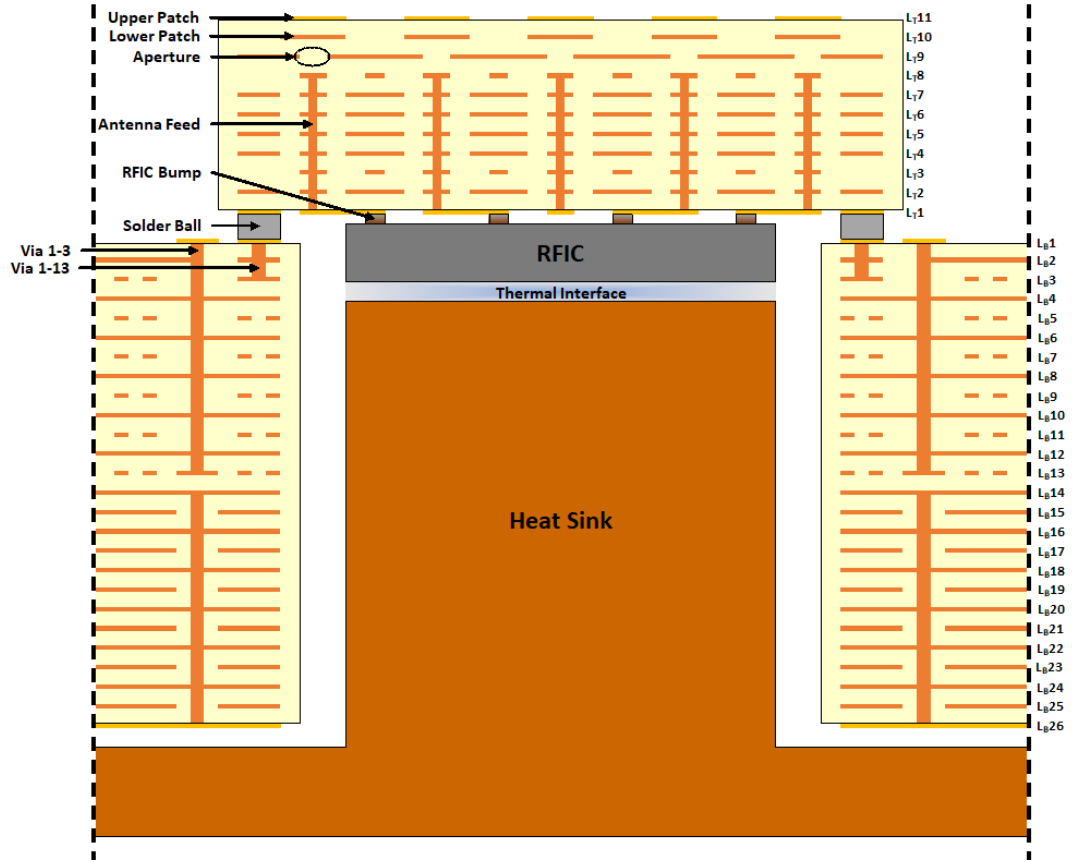
- ASP Antenna is constructed using PCB HDI technology
- RFIC fan-out, via transition, antenna feed, resonant aperture and stacked patches form compact vertical stack-up
- Easily configured as λ/2-spaced antenna array for use with scalable phased arrays

384-Element W-Band Phased Array System



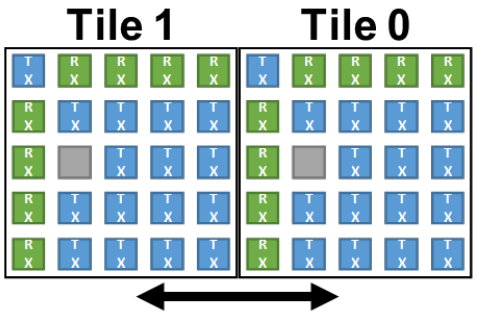
[S. Shahramian et al. JSSC 2019]

Antenna-in-PCB Stack Overview

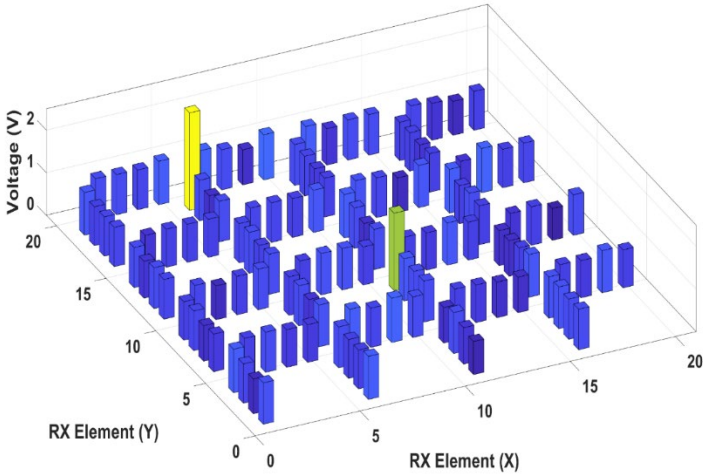


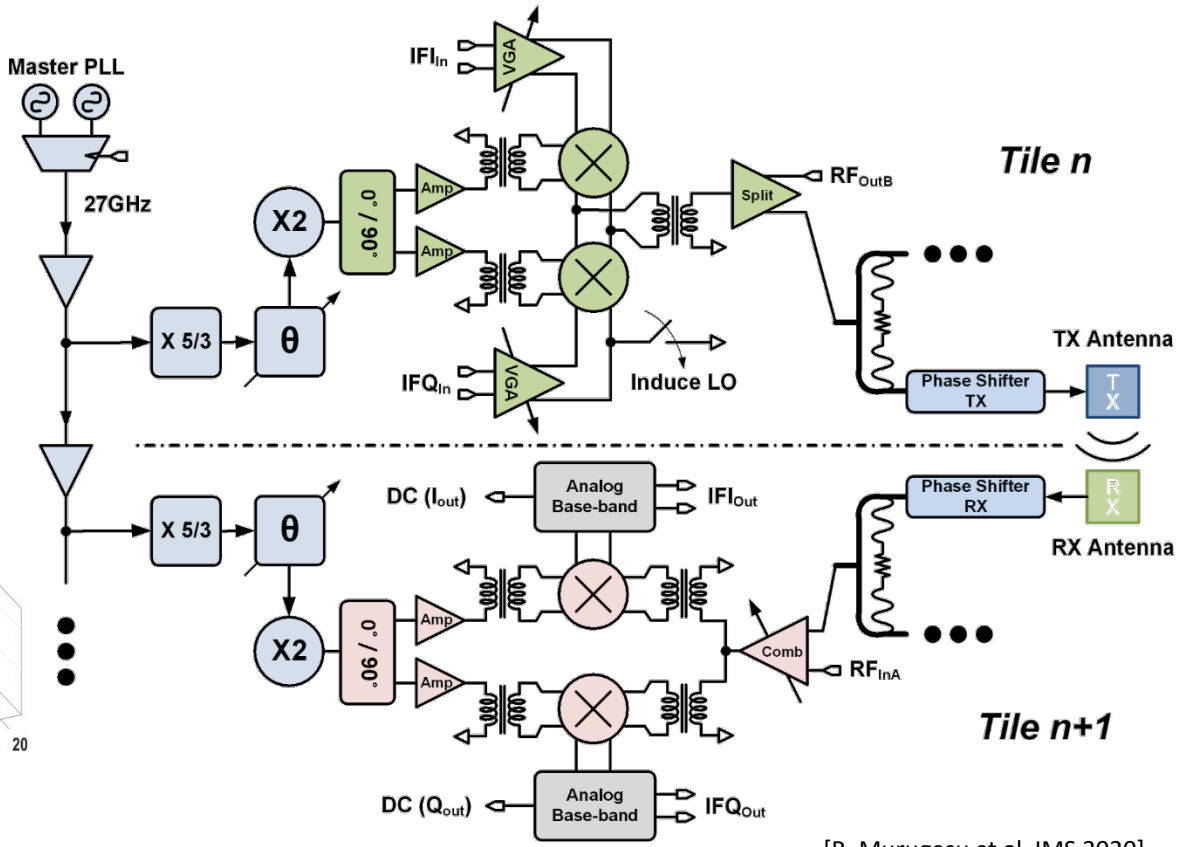
- Full organic stack including main carrier PCB
- Matched thermal co-efficient between critical interfaces
- Stack complexity is driven by RFIC complexity and W-band signal integrity requirements
- Ensuring uniform antenna spacing across multiple tiles is challenging!

Leveraging Undesired Coupling Effects



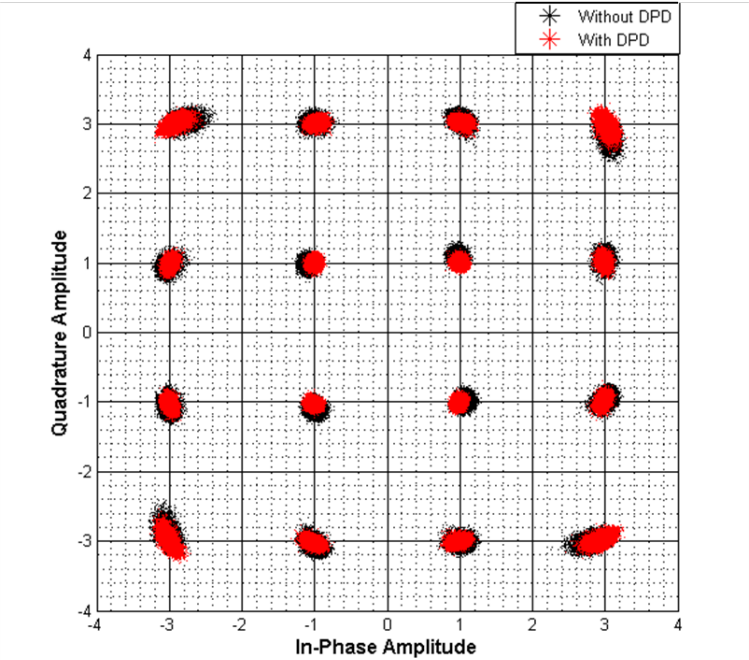
Parasitic TX ⇔ RX Coupling





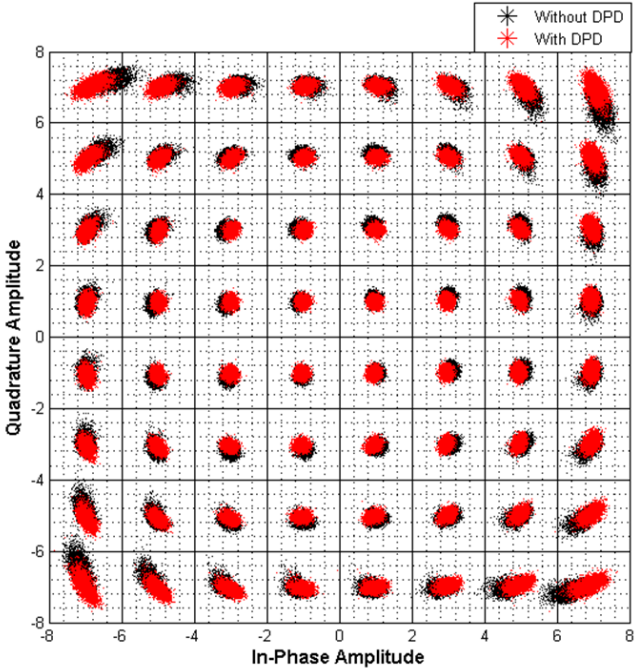
[R. Murugesu et al. IMS 2020]

Using Antenna-to-Antenna Coupling to Train DPD



Wireless Link Improvement

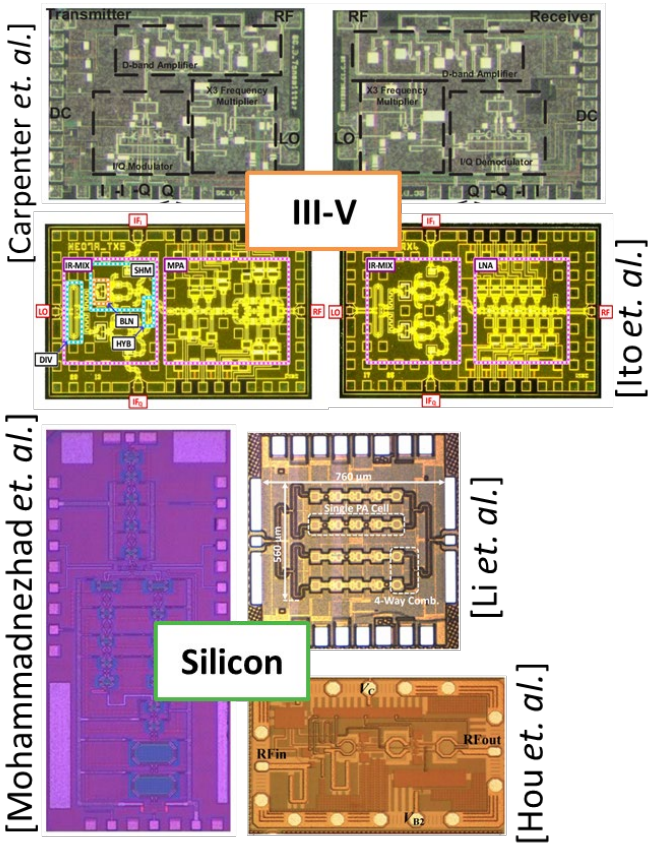
- 16-QAM at 2.5GB/s (10Gb/s)
- EVM improvement -25.4dB ➔ -30.5dB

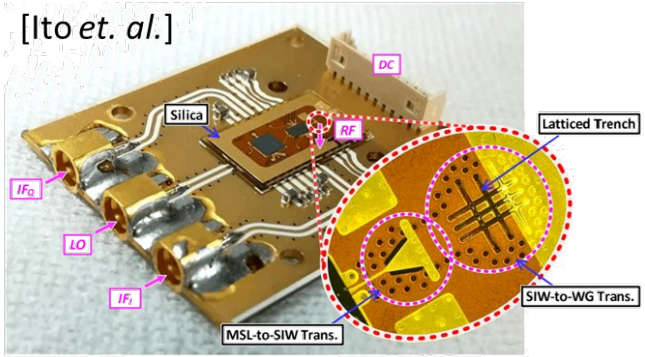


Wireless Link Improvement

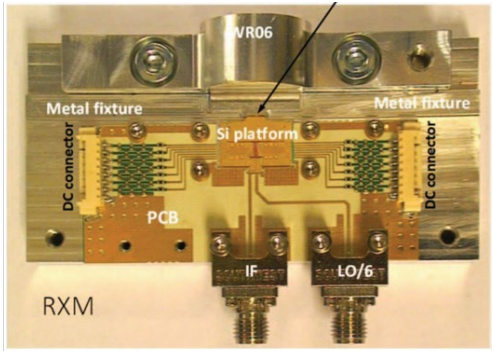
- 64-QAM at 2.5GB/s (15Gb/s)
- EVM improvement -27dB ➔ -31dB

Challenges of near-THz Module Design

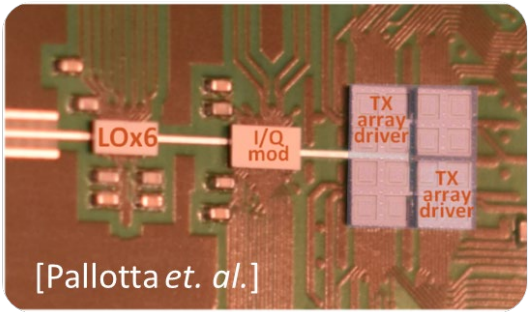




- SIW to Waveguide Transition on silica-based substrate
- **Loss = 1.75dB**

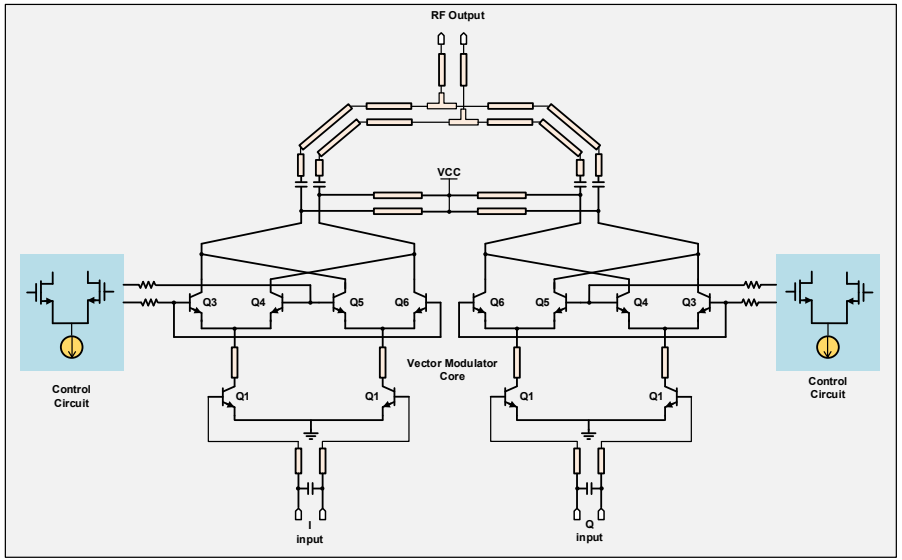


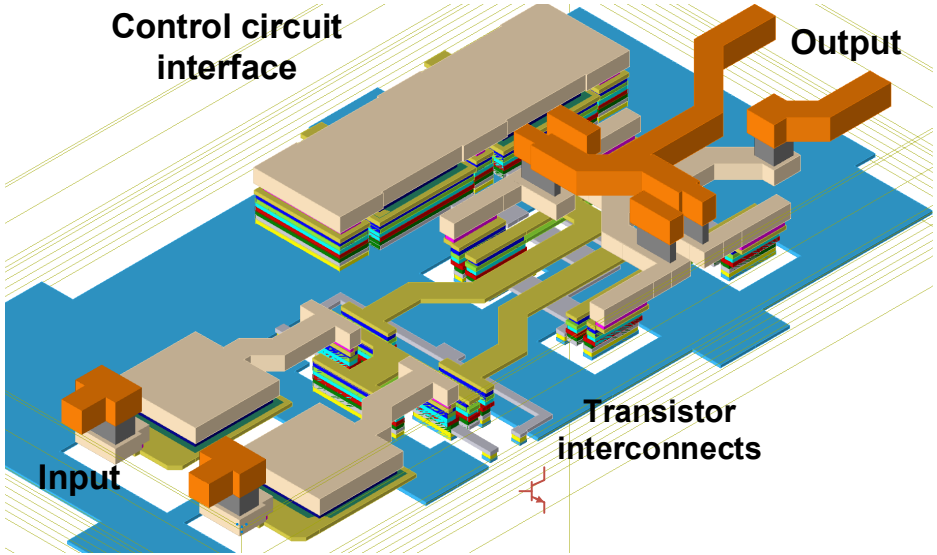
- On-chip slot radiator mounted in the waveguide's H-plane
- **Loss = 4.4 – 5.5dB**



- PCB-based cavity-backed aperture-coupled patch antennas (ACPA)
- **Loss = > 3dB**

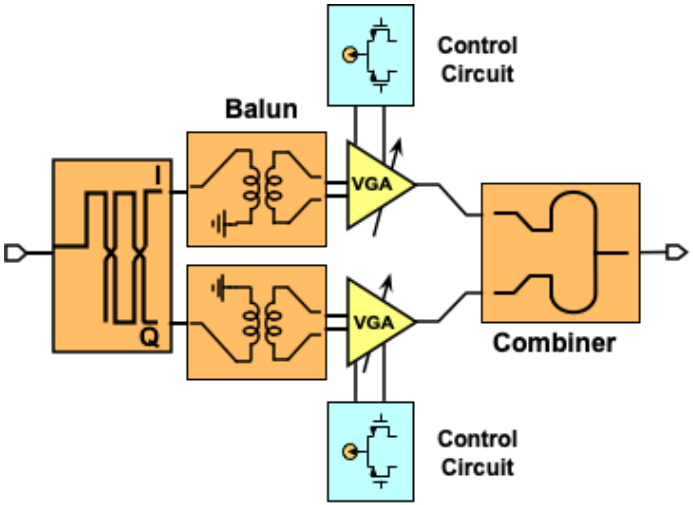
Active Elements in near-THz Circuits

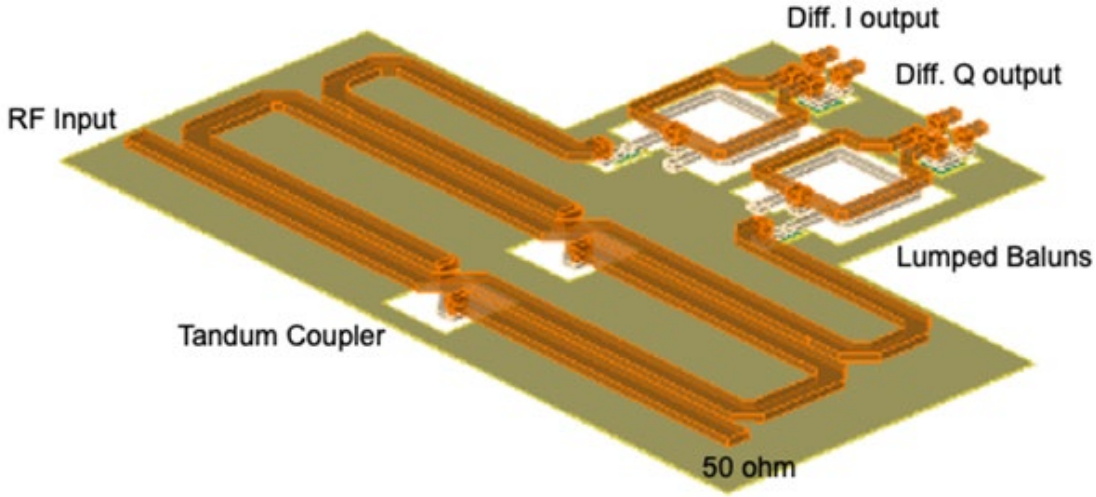




- Gilbert-cell based VGA operating at 160GHz for use in phased array phase shifter
- Complete core layout EM extraction including surrounding GND planes & bias lines
- Note microstrip output matching network

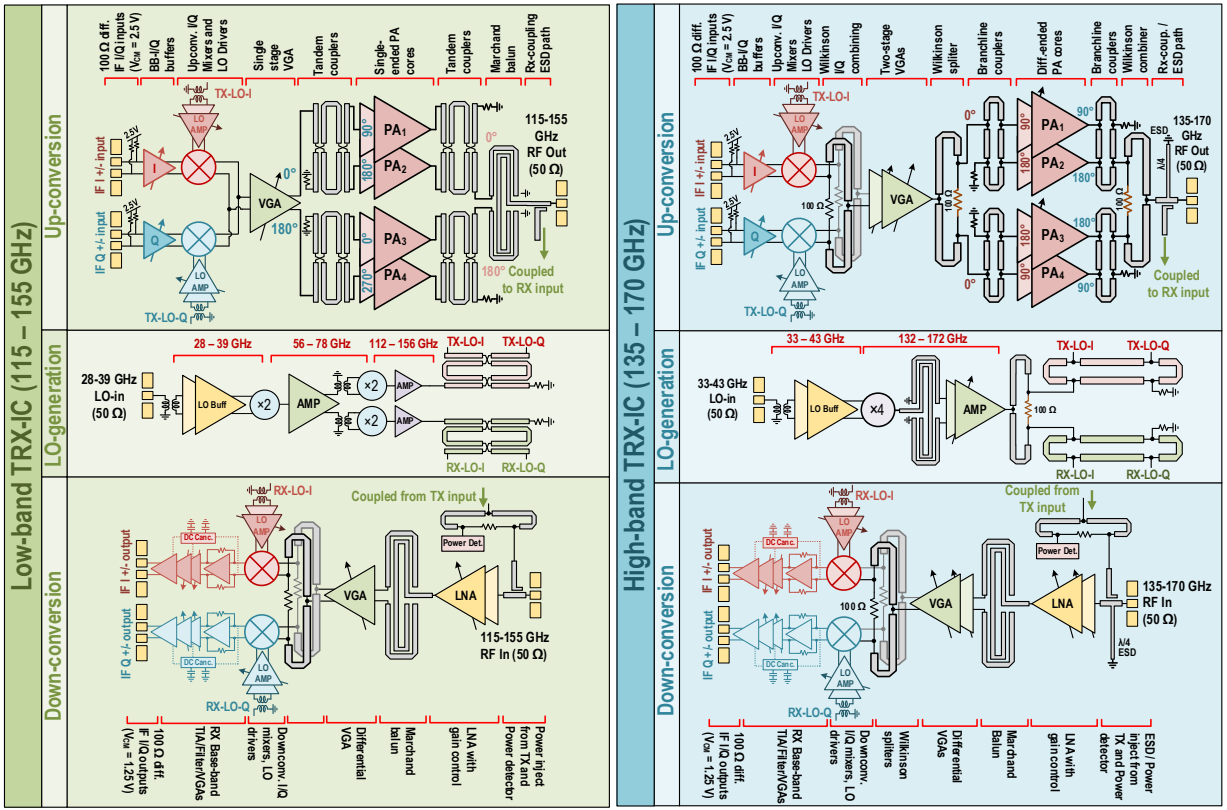
Hybrid Passive Structures at near-THz





- A combination of lumped (transformers) and distributed (tandem coupler) is used
- The combined structure is simultaneously EM extracted and simulated
- Simulated phase imbalance <2° and amplitude imbalance of ±0.6dB at 150GHz

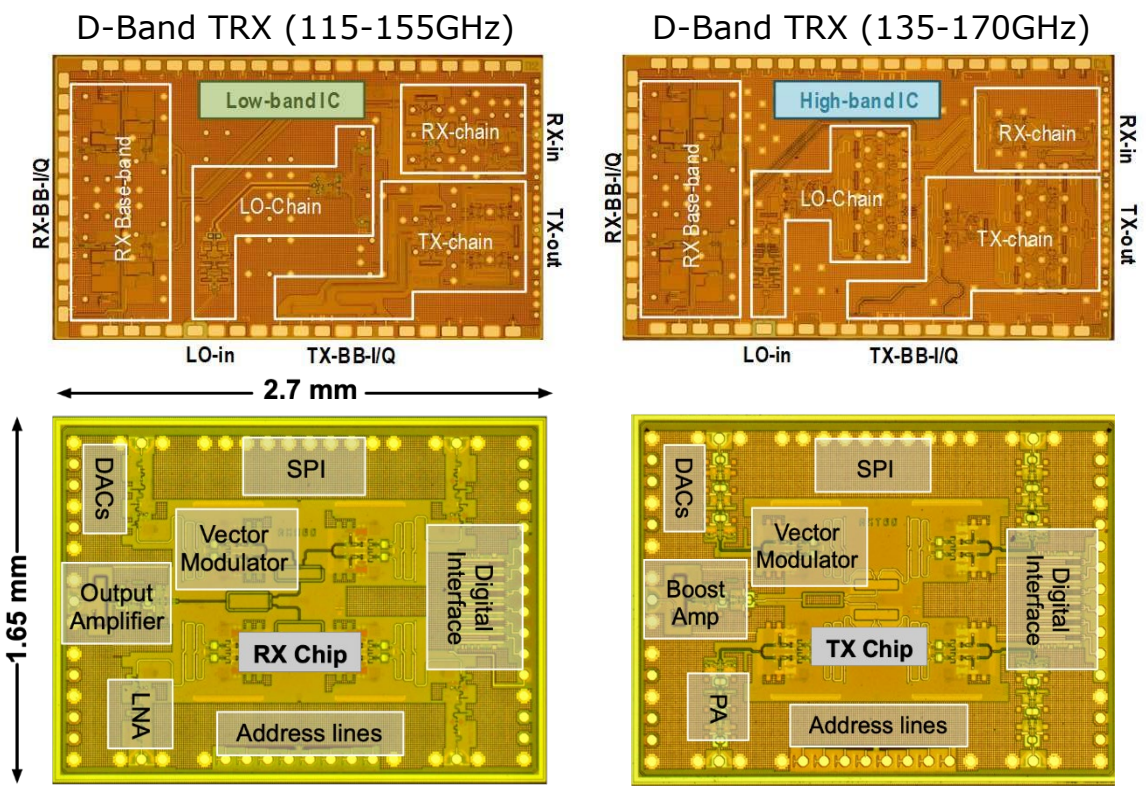
D-Band is the new E-Band!



- The complexity of state-of-the-art D-Band (and near-THz) RFICs resembles that of mm-wave ICs!
- Fully integrated with calibration, self-test, analog baseband, LO networks, etc.
- Directly interface to digital modem chipset without any external components

[A. Singh et al. RFIC 2020]

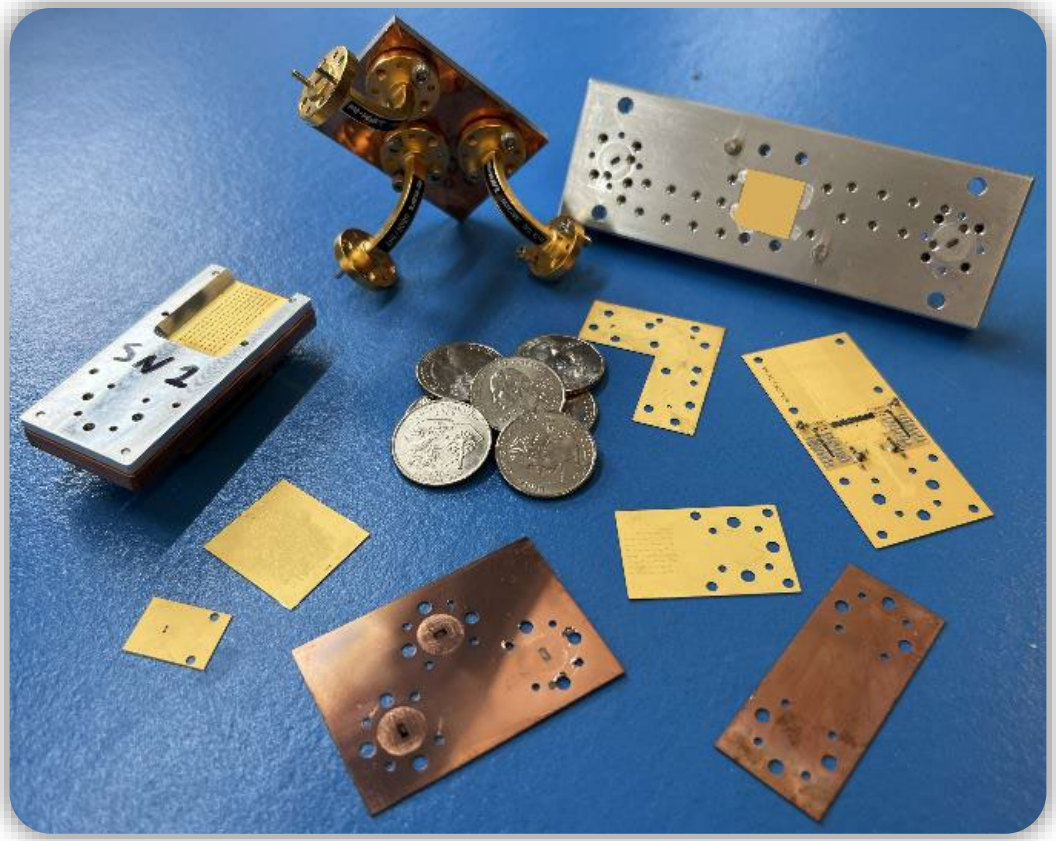
D-Band Chipset Family



- IHP SG13G2 130 nm SiGe BiCMOS (f_T / f_{MAX} of 300/500 GHz)
- Dimensions of D-Band phased array RFICs can easily exceed the required λ/2 spacing
- Creative layout techniques and component choices are required for optimized chip dimensions

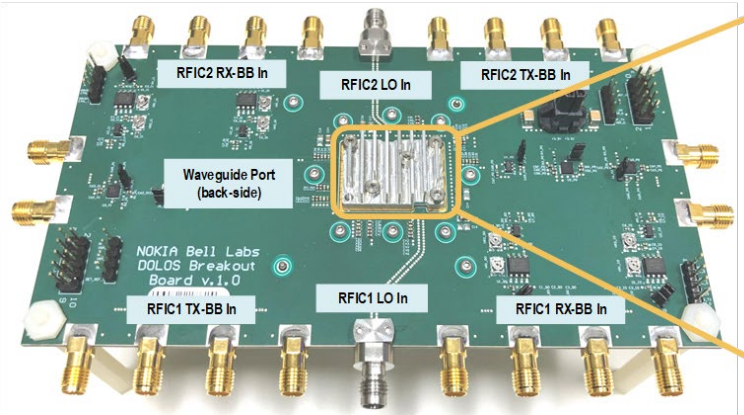
[M. Elkhouly et al. ISSCC 2022]

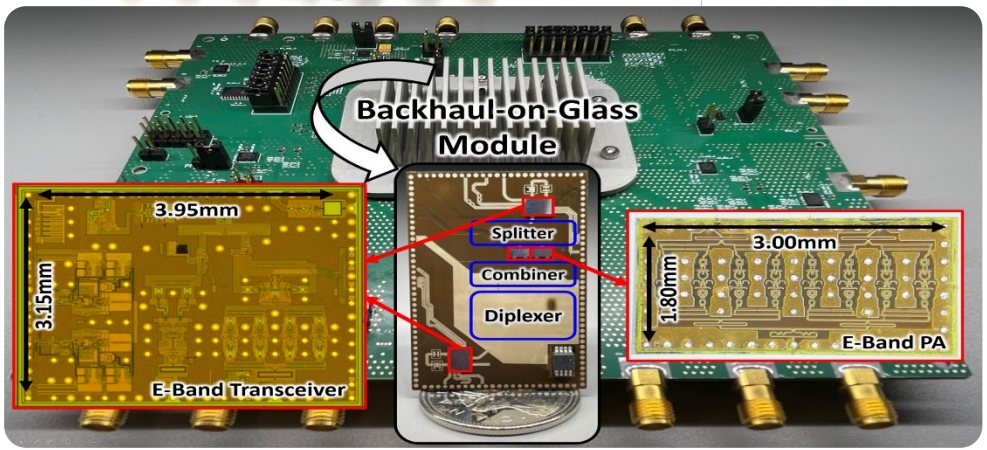
Glass Substrate Exploration



- A wide range of glass components designs have been explored
- A diverse set of transitions, flip-chip pad frames, filters, antenna arrays and diplexers test structures have been fabricated and tested
- Refined models and interposer characteristics have been established which allows complex modules to be realized with high confidence

Radio-on-Glass Modules (D- & E-Bands)

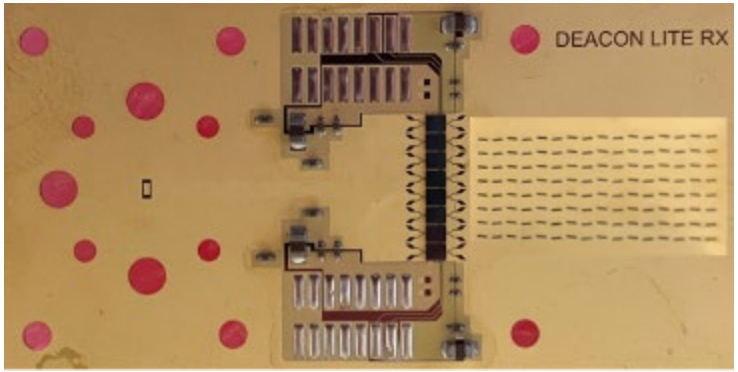


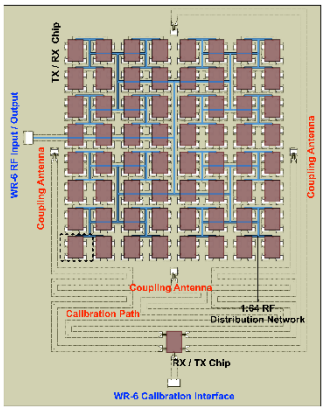


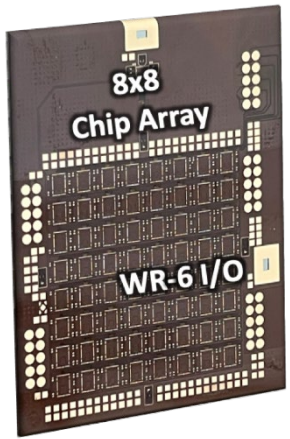
- Glass interposer is considered as the extension of the RFIC's BEOL due to the fine lithography features of the process
- Each material (Silicon, Glass, PCB) is leveraged for its strengths. PCB does not carry any D- or E-Band signals
- Record module performance has been demonstrated

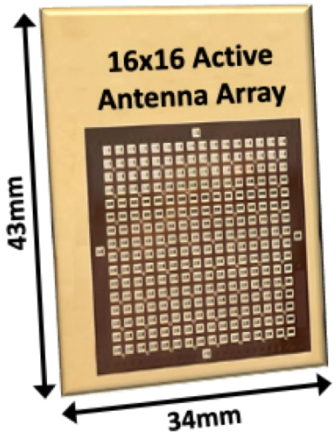
[S. Shahramian et al. RFIC 2022]

Phased-Array-on-Glass Modules (D-Band)









- 1D and 2D phased arrays are realizable on glass interposer using multi-element RFICs
- 2D phased arrays architecture is fully scalable both at RFIC & interposer level
- Record module performance has been demonstrated

[M. Elkhouly et al. ISSCC 2022]

Concluding Remarks

- Designers continue to push the boundaries on vertical integration
  - Fully integrated near-THz RFICs with advanced built-in functions
  - Co-designing integrated circuits and packaging regardless of stack or material

- Our ambitions for next generation systems always lead our computational power
  - Mastering the art of mm-wave & near-THz layout is a valuable asset in bringing next generation products to market
  - Complex mm-wave chipsets with several designers demand careful communication and collaboration between designers, circuit level, ASIC layout level & module integration stage