EECS 240B
Advanced Analog Integrated Circuits
Lecture 3: Passives

Jun-Chau Chien

with Ali M. Niknejad, Osama Shana'a

Spring 2024

Passive devices

Summary

- **Resistors**
- **Capacitors**
- **Inductors**
- **Diodes**
- **BJT**

Resistors

Resistors types

- Silicide resistors

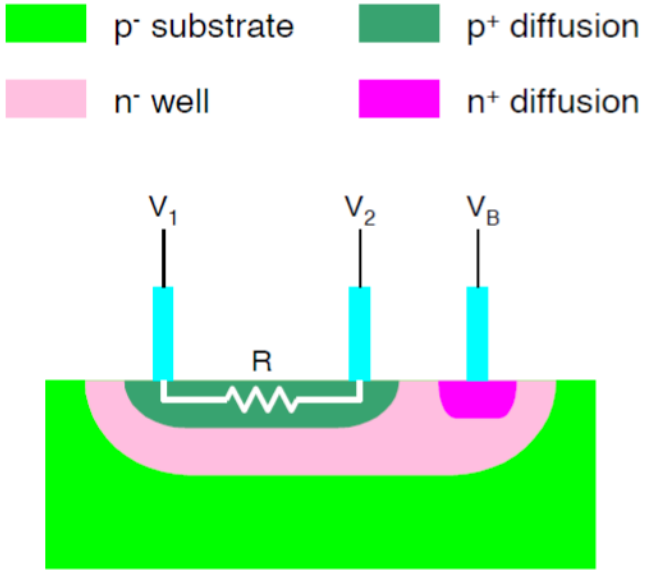
Layer	Sheet resistance
Aluminum	60 mΩ/□
Polysilicon	5 Ω/□
N+/P+ diffusion	5 Ω/□
N-well	1 kΩ/□

- Non-silicide (higher sheet resistance)

Layer	R/□ [Ω/□]	T_C [ppm/°C] @ T = 25 °C	V_C [ppm/V]	B_C [ppm/V]
N+ poly	100	-800	50	50
P+ poly	180	200	50	50
N+ diffusion	50	1500	500	-500
P+ diffusion	100	1600	500	-500
N-well	1000	-1500	20,000	30,000

- Absolute resistance values varies by +-20%
  - Trimming needed if accuracy is of concern
- Temperature coefficient (TC, ohm/°C)
- Voltage coefficient (VC, ohm/V)
- Can mix different types to create zero-TC resistor

P+ diffusion resistor



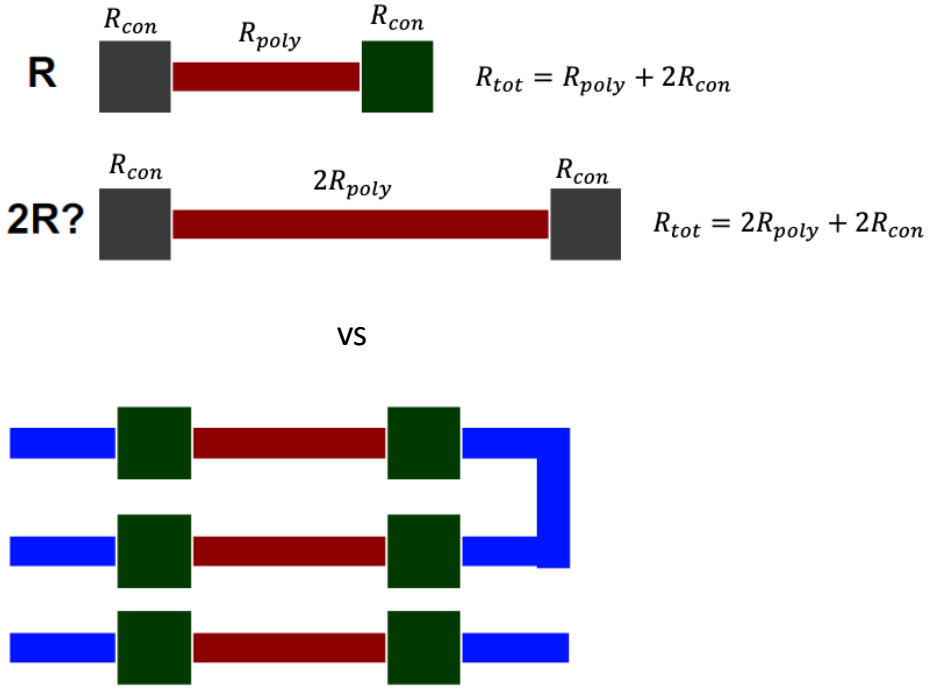
Silicide

- Ion implantation to lower the resistance of source/drain and polysilicon material.
- Titanium silicide ($TiSi_2$) is widely used saclide (self-aligned silicide), low resistivity (13-17 Ω-cm) and high melting temperature (1540°C).
- Another widely used is $CoSi_2$ and PtSi.

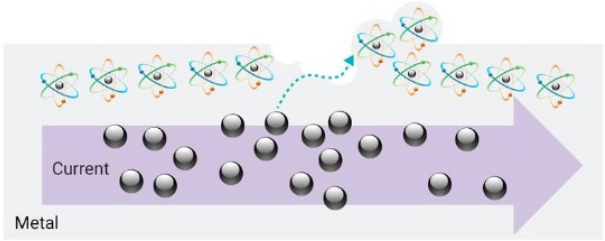
Resistors

Variations and mismatches

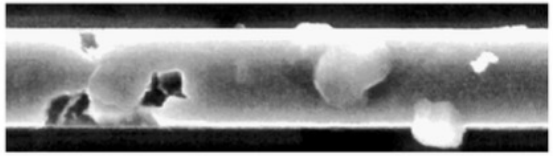
- Systematic, e.g. need a R and 2R.
- Batch variation
- Mismatches
  - Current direction matters!



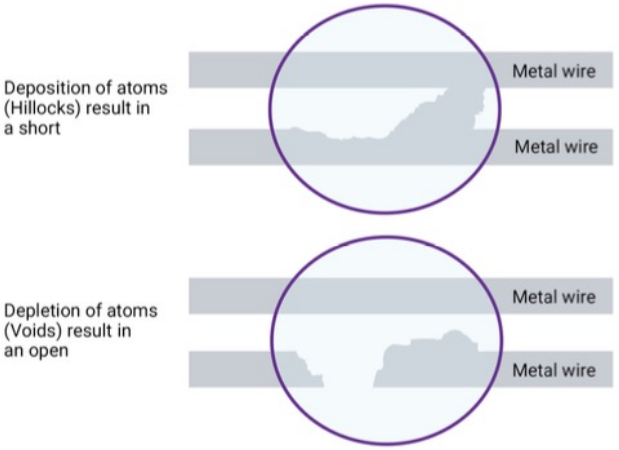
Electron migration



Courtesy of Synopsis



Worst case…



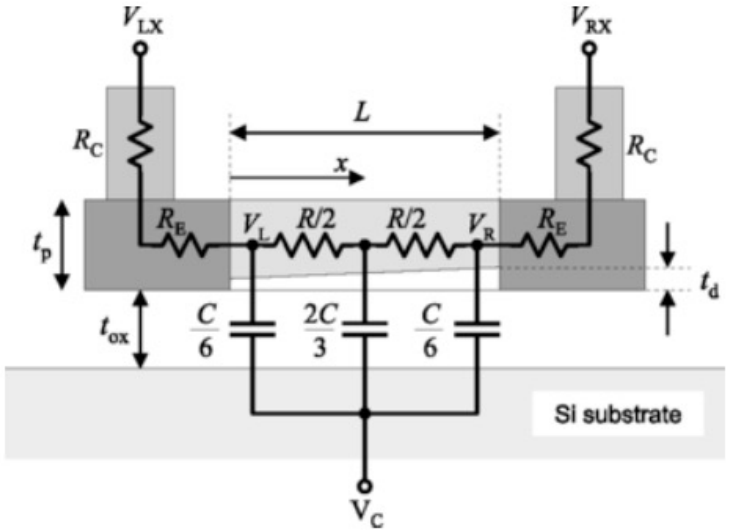
Need to make sure wire width is enough to handle electron-migration current density rules

Resistance changes over time
as a function of current density (mA/µm),
DC or AC (r.m.s), temperature

Check current density requirement (in DRM) offered by foundry, and put those equations into an excel sheet for calculation.

- Electron migration is related to current density flow within a metal.
- If the current density is high enough, the heat dissipated within the material will repeatedly break atoms from the structure and move them. This will create both ‘vacancies’ and ‘deposits’. The vacancies can grow and eventually break circuit connections resulting in open- circuits, while the deposits can grow and eventually close circuit connections resulting in short-circuit.

Resistors
Model



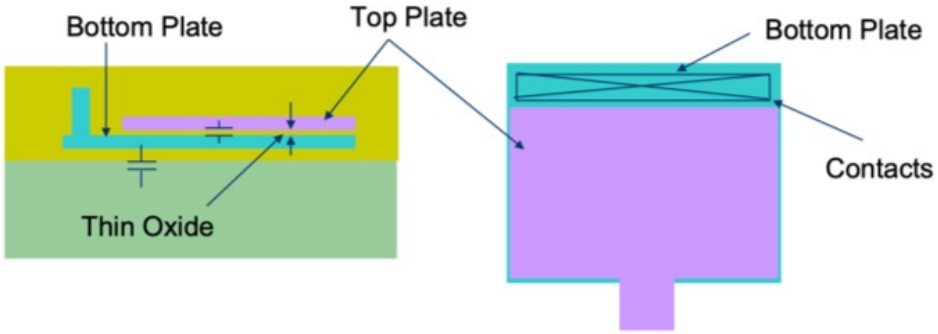
- Polysilicon resistors can have depletion due to electrostatic, causing resistance variation.
- My personal preference is “p+ poly”, to have same type as the silicon substrate.
- Make sure to include parasitic capacitance in your design (degrade bandwidth), included in the post-layout extraction.
- Use width > 2 µm if absolute resistance is of concern. Experience 20% drop even with w = 10 µm…
- Make sure to include dummy resistor on each side to avoid under-cut during the lithography.
- Resistors can have ”flicker (1/f)” noise, this is not always included in the model (some in RF model, but accuracy is questionable…).

Capacitors

Capacitor

Basics

Capacitor
Implementation



Model

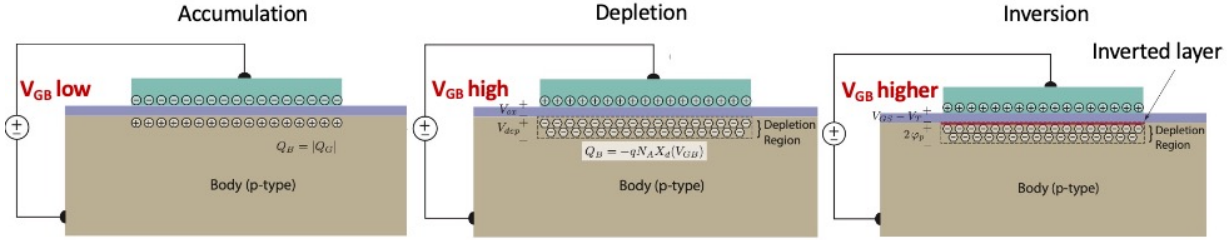
Capacitor

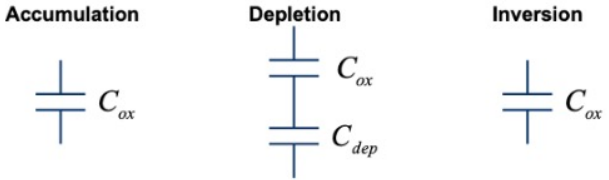
Summary of all options

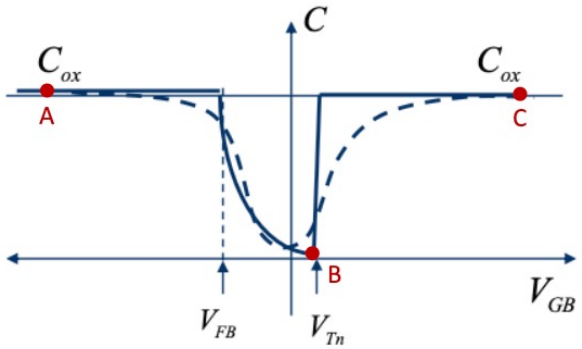
Type	C [aF/μm²]	V_C [ppm/V]	T_C [ppm/°C]
Gate (thick oxide)	8000	Huge	Big
MIM (option)	4000		
MOM (> 5 metals)	~2000		
Poly-poly (option)	1000	10	25
Metal-metal	50	20	30
Metal-substrate	30		
Metal-poly	50		
Poly-substrate	120		
Junction capacitors	~ 1000	Big	Big

Capacitor

MOScap

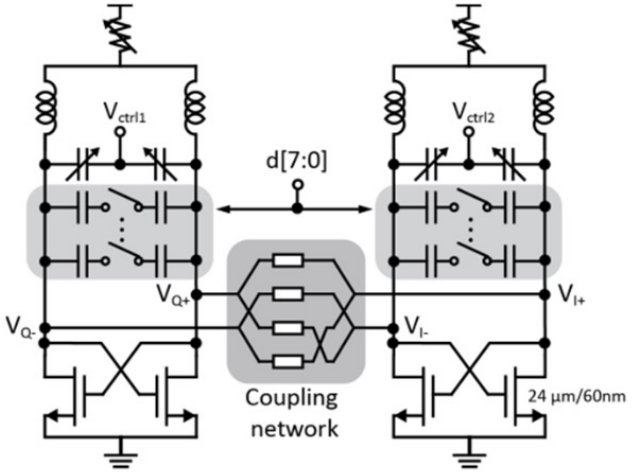




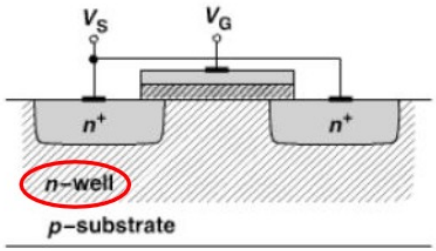


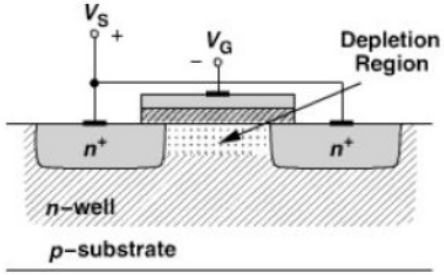
Variable capacitor (or varactor)

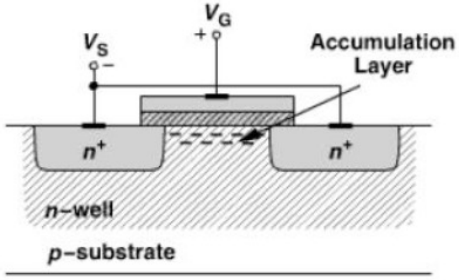
RF voltage-controlled oscillator (VCO)

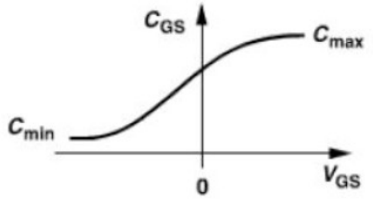


Accumulation-mode MOS (A-MOS, or NMOS-in-Nwell)



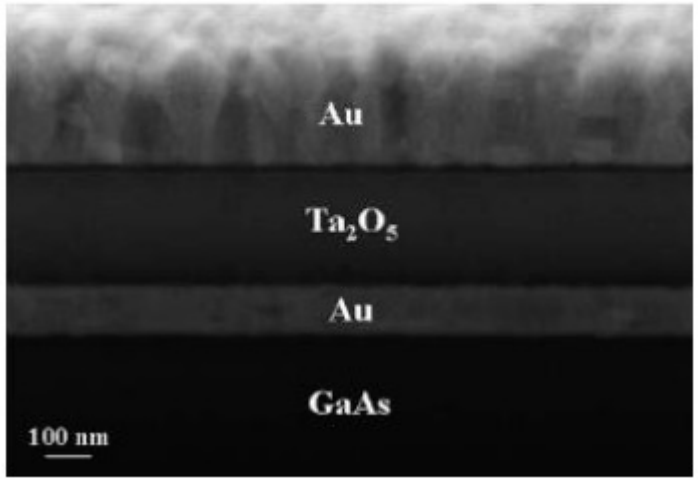




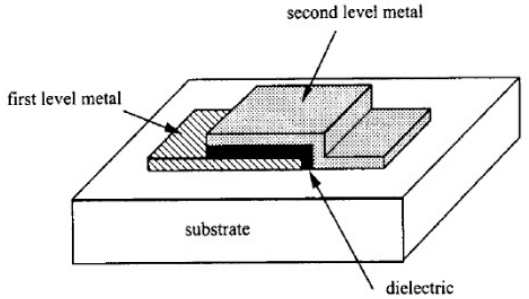


MIMCap = Metal-insulator-metal capacitor

Not all processes have such an option…



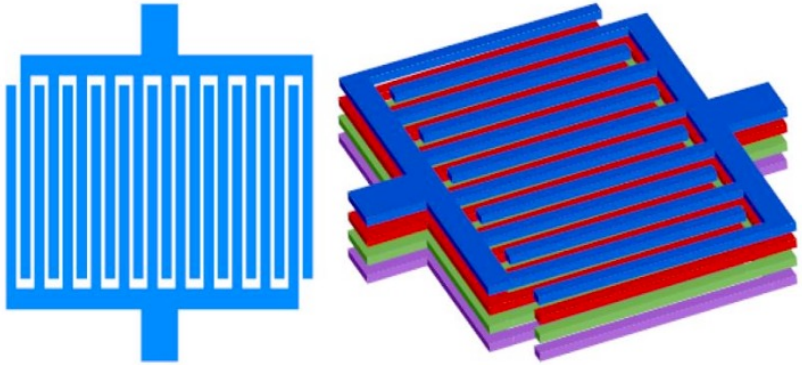
25 nm thin dielectric

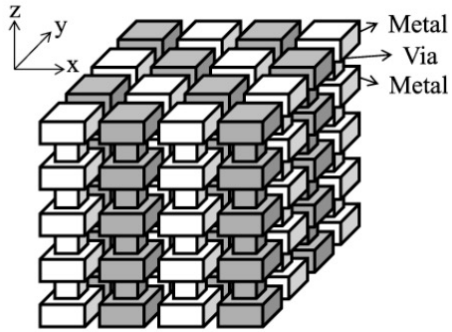


Offered in CMOS 180nm at 1~2 fF/um^2 but not the others per experience.

MOMcap = Metal-oxide-metal capacitor

Come for free!





- Capacitance density: 1~3 fF/μm^2, lithography dependent.
- Watch out for the breakdown voltage.
- “CRTMOM” is pretty popular (interleaved with 90° rotation); can do custom post-layout extraction (pretty accurate compared to EM-simulation)
- Watch out for the parasitics, CMOS 90nm: 5%, CMOS 28nm: 1% (1% is a really good number!)
- Can bundle with MOScap and MIMcap as a high-density cell for supply decoupling unit.

Capacitor layout

Always employ unit cell and translational matching

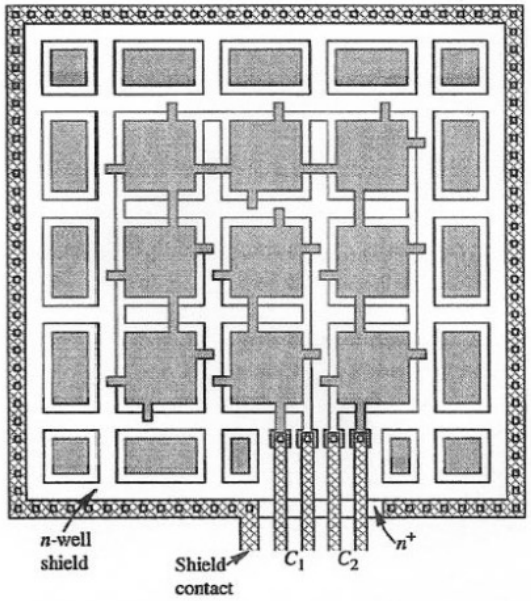


Figure 6.17 A layout of two capacitors with ratio $C_2/C_1 =$ ⅓, incorporating several of the techniques discussed in the text (adapted from Ref. 23).

- Unit elements
- Shields:
  - Etching
  - Fringing fields
- "Common-centroid"
- Wiring and interconnect parasitics

Ref.: Y. Tsividis, "Mixed Analog-Digital VLSI Design and Technology," McGraw-Hill, 1996.

Capacitor
Model

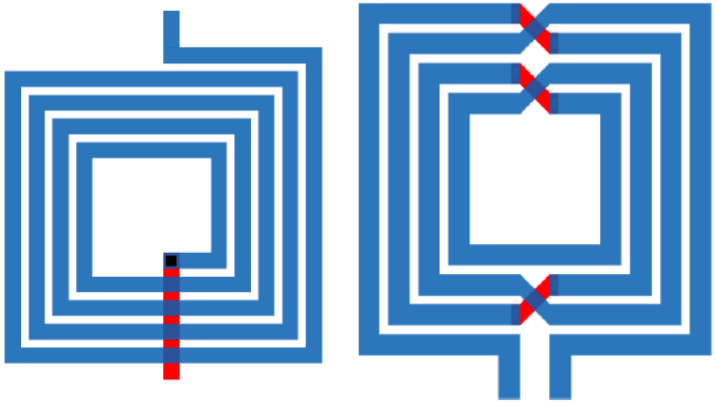
- A 3-terminal distributed model.
- Rs represents series resistance of metal layers comprising the MoM structure.
- Csub1,2 and Rsub1,2 represent bottom plate caps to substrate and loss.
- Cs is MoM cap value including fringing.
- Include series inductor to model phase shifts at very high-frequency (> 30 GHz).

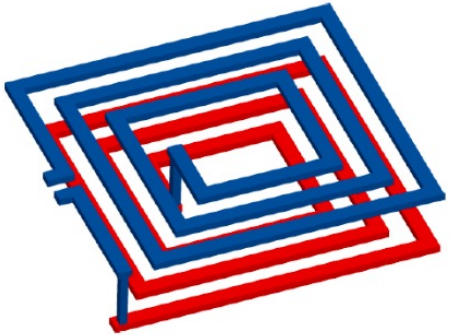
Inductors

Inductors
Basics

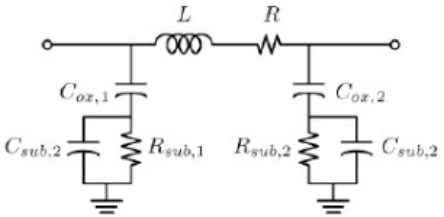
Inductors

Layout



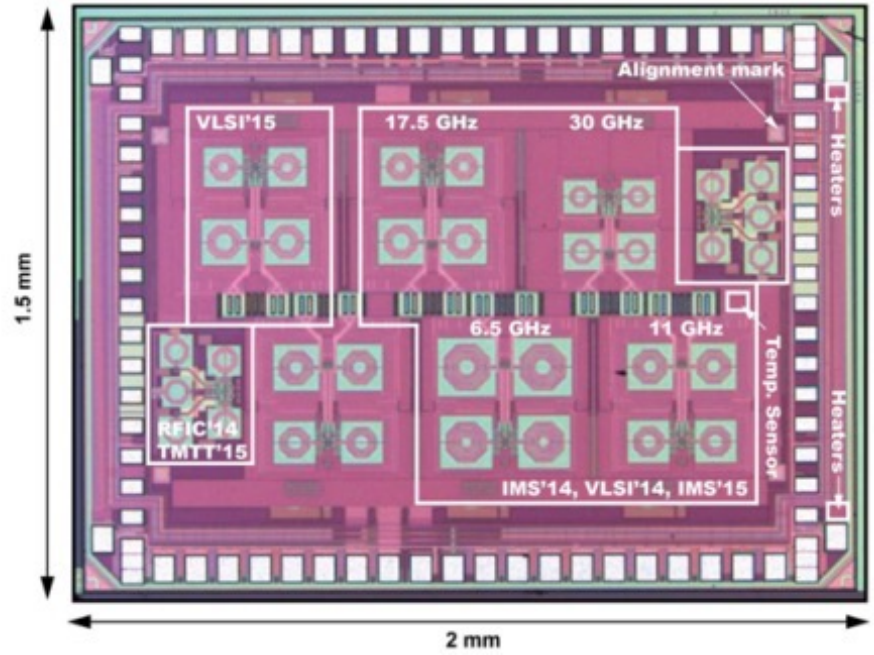


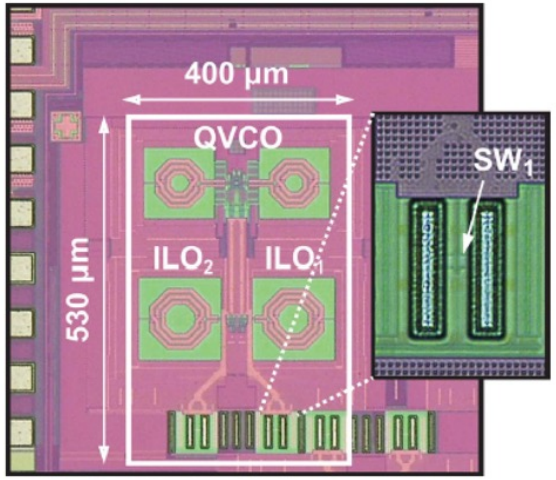
Lumped model



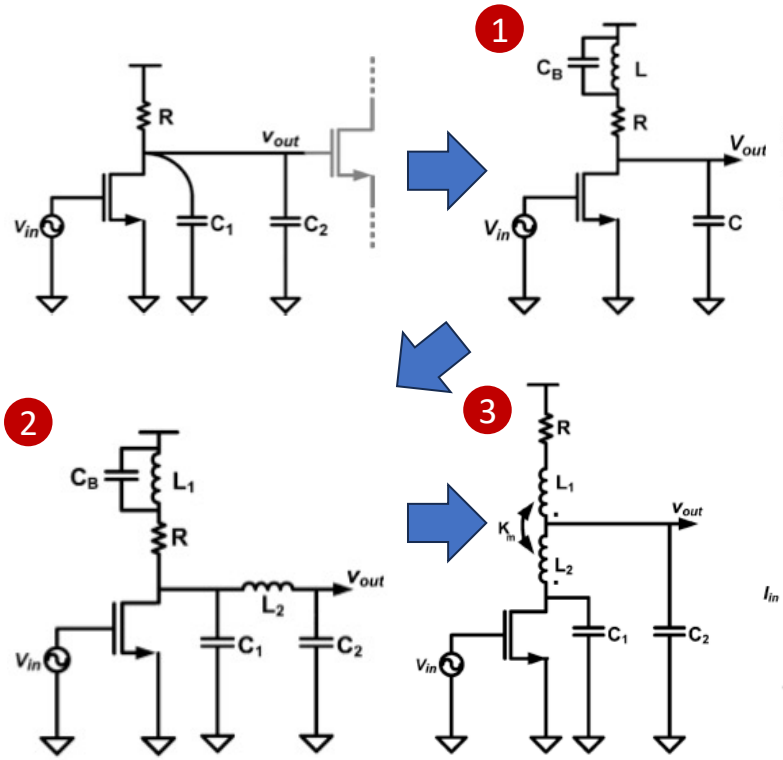
- **Widely used in RF designs, L ranges from 30 pH ~ 10 nH depending on the frequency, e.g. 500 MHz ~ 300 GHz**
- **Implemented with top metal layers**
  - **Usually thick metals for power distribution, can be as thick as 4 µm**
  - **Away from substrate to avoid high parasitics capacitance**
  - **Si substrate must be "undoped" one (resistivity = 10 ohm-cm) to minimize losses**
  - **Requires E&M simulation (solving Maxwell Equations); usually the inductance is very accurate but Q requires iterations**

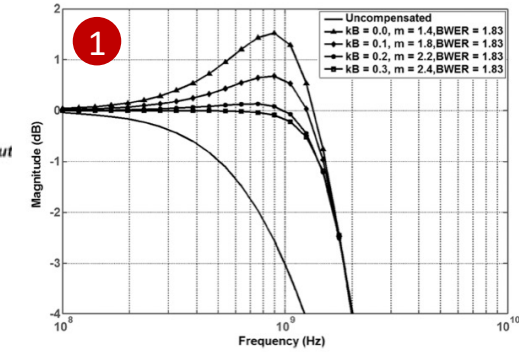
Example

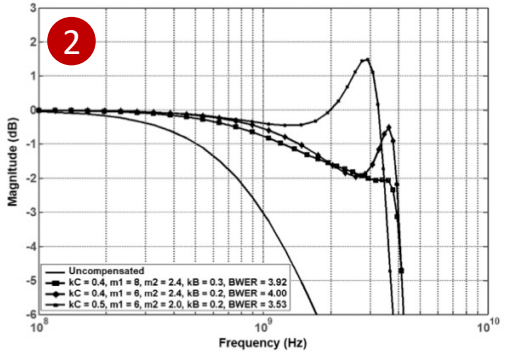

Alignment mark
VLSI'15
17.5 GHz
30 GHz
Heaters
6.5 GHz
11 GHz
Temp. Sensor
RFIC'14
TMTT'15
IMS'14, VLSI'14, IMS'15
Heaters
1.5 mm
2 mm

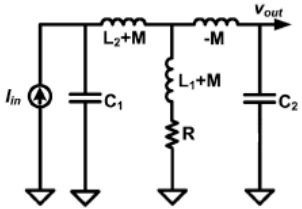

400 µm
QVCO
SW1
ILO2
ILO1
530 µm

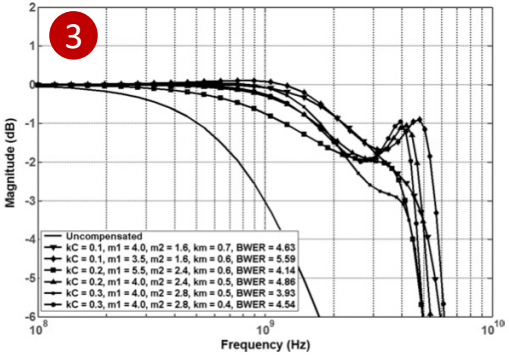
Shunt peaking for bandwidth extension







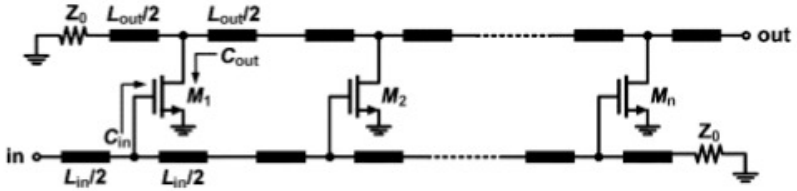




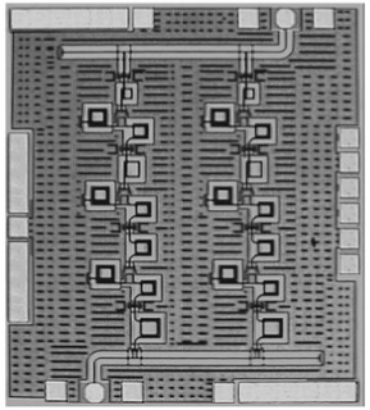
Shekhar, Bandwidth Extension Techniques for CMOS Amplifiers, JSSC'06

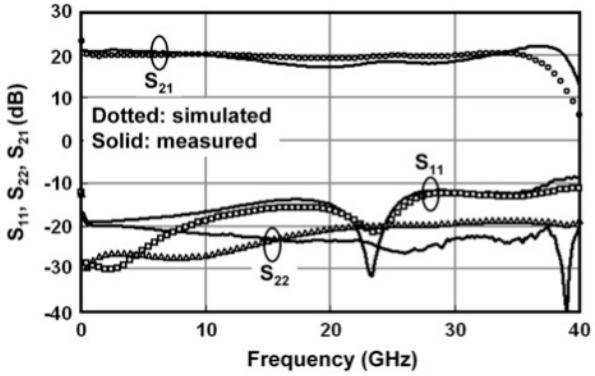
Further distribution of capacitance

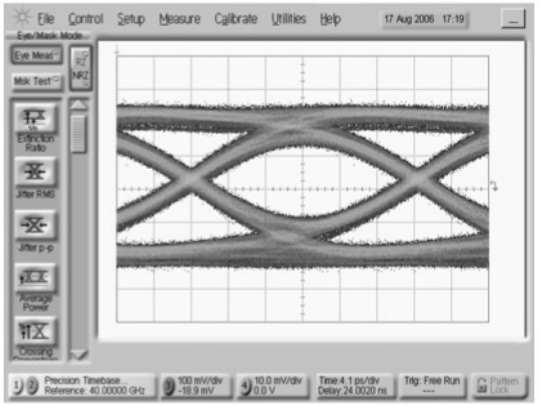
Distributed amplifier



20 dB, 39.4 GHz in 180-nm CMOS with f_T = 50 GHz





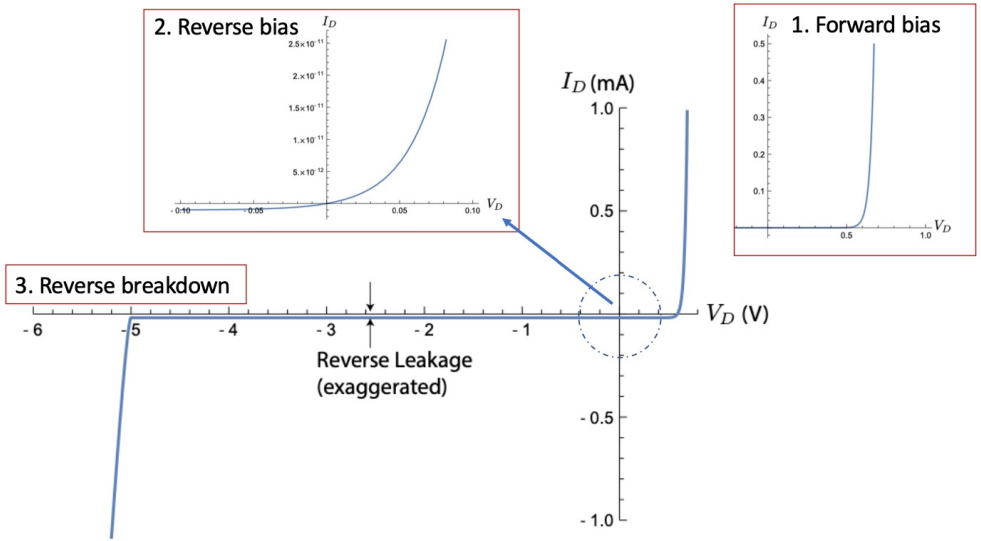


Chien, ISSCC'07

Diodes

Diodes

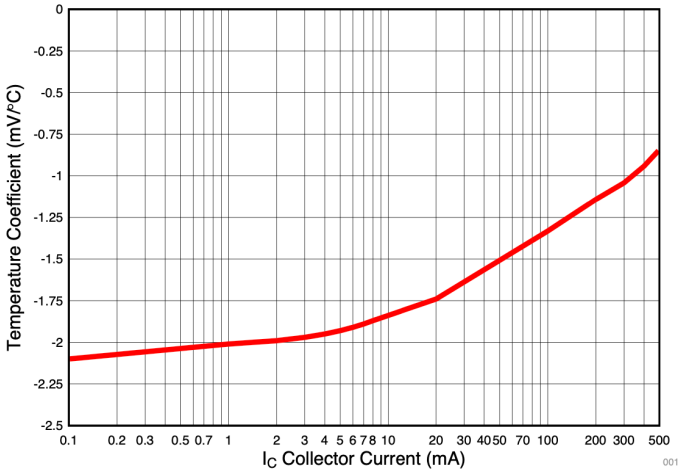
I-V characteristics



$$I_D = I_S\left(e^{\frac{V_D}{V_T}} - 1\right),$$

$$V_D = \frac{kT}{q} ln\left(\frac{I}{I_S}\right)$$

$$\frac{\partial I_S}{\partial T} = 0.1\ pA/K$$



Source: TI App Note

Diodes of various types

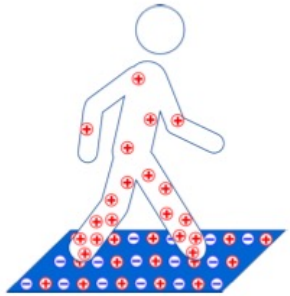
Cross-section view and layout

P+/Nwell

N-well/PSUB

N+/PSUB

ESD protection



ESD testing standards

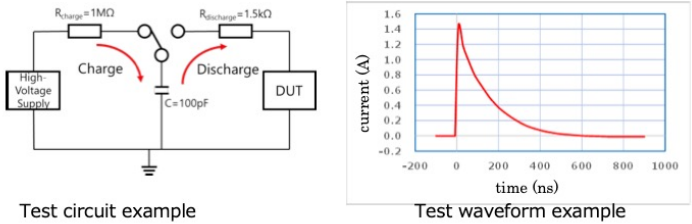


Figure 2.3 Human body model (HBM)

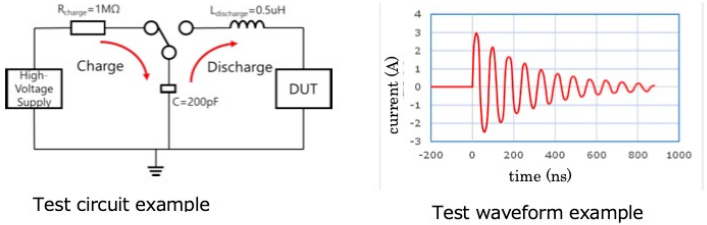


Figure 2.4 Machine model (MM)

https://toshiba.semicon-storage.com

- ESD by itself is a dedicated research topic!
- In the company, there will be a dedicated ESD team for the management and testing.
- There are specific I/O pads with ESD cells offered by the foundry.
- Do not ignore its parasitics capacitance!

BJTs

Both NPN and PNP possible

Cross-section view and layout

Vertical PNP (vpnp)

Horizontal NPN (need triple-well process)

- β ~ 10, relative low speed due to wide base. Mainly for bandgap reference.
- Mostly PNP in CMOS.